

026-4

Front View

129	1	Video controller	✓	Components →
129	2	Video RAM (20 conn) ^{next} + ECL/RPU	✓	
	3	Remote (30 conn) ^{RCmd}		600M + ±12
129	4	CPU (50 conn)	✓	
	5	PS DC/DS + jumper (20, 30, 50 conn) ^{S/E KB CPU}		CIC-6
129	6	CIC-6 Interface (40 conn) ^{CIC-6}		Remote

129
J1, 2, 4, 5-4

Prototype

Components ←

1. ECL + RPU serial, Video RAM
2. Remote
3. CRT Controller
5. CPU
7. PS + Interconnect
8. CIC-6 Int

5M

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

4

PASS 1

MIN.	SEC.	ERRS
15	16	

PASS 2

MIN.	SEC.	ERRS
26	50	

PASS 3

MIN.	SEC.	ERRS
38	25	

PASS 4

MIN.	SEC.	ERRS
49	59	

PASS 5

MIN.	SEC.	ERRS
61	33	

PASS 6

MIN.	SEC.	ERRS
73	8	

PASS 7

MIN.	SEC.	ERRS
84	42	

PASS 8

MIN.	SEC.	ERRS
------	------	------

COMPUTER IMAGE TERMINAL
SPECIAL CHARACTERS RECEIVED BY TERMINAL

DG CONTROL	ESCAPE SEQUENCE	FUNCTION
G		BELL
L	J	CLEAR PAGE
	J	CLEAR TO END OF PAGE (INC. CHARACTER AT CURSOR)
K	K	CLEAR TO END OF LINE (INC. CHARACTER AT CURSOR)
N	RA	START BLINK FIELD
O	RG	END BLINK FIELD
W	A	CURSOR UP
Z	B	CURSOR DOWN
Y	D	CURSOR LEFT
[		TRANSMITS ESCAPE
J		LINE FEED
X	C	CURSOR RIGHT
H	H	CURSOR HOME
E		CURSOR POSITION REPORT
	[	CHANGE BAUD RATE 1
	\	CHANGE BAUD RATE R *SEE PAGE 2
	a	SEND CURSOR POSITION TO HOST
	Y<LINE><COL>	SET CURSOR POSITION
	&	SET ALL LIGHTS OFF
	'	SET ALL LIGHTS ON
	"<H><H>	SET 1 LIGHT OFF
	#<H><H>	SET 1 LIGHT ON
	\$	REPORT LIGHTS OFF
	%	REPORT LIGHTS ON
	b	DISABLES CONTROL PANEL
	c	ENABLES CONTROL PANEL
	S	SEARCH AND CLEAR BLINK FIELD
	T(*)	SET ERROR CHARACTER * *=A-I
	U	CLEAR MATRIX ERRORS
	V	CLEAR ERROR LINE
	W(####)	OUTPUT ERROR #
	X(#)	OUTPUT VIDEO RATE #=0-3
	Y(#)	OUTPUT DIMENSION #=0,1

NOTE: There are two ways to produce many of the control functions such as clear page, etc. One emulates Data General terminals, the other Teleray. The terminal will respond at all times to either. The codes produced by the keyboard are Data General standard. Control codes are single key codes whereas ESCAPE sequence begins with ESCAPE followed by a sequence.

<H>=HEX DIGIT 0-F

*CHANGE BAUD RATE TO ECLIPSE OR TO RPU CONTROLLER

*ESC [# - CHANGE BAUD RATE TO ECLIPSE

*ESC \# - CHANGE BAUD RATE TO RPU

*WHERE # IS AN ASCII CHAR DEFINED AS FOLLOWS

*	# = 0	THEN BAUD =	16 X EXTERNAL CLOCK
*	# = 1	THEN BAUD =	50
*	# = 2	THEN BAUD =	75
*	# = 3	THEN BAUD =	110
*	# = 4	THEN BAUD =	135.5
*	# = 5	THEN BAUD =	150
*	# = 6	THEN BAUD =	300
*	# = 7	THEN BAUD =	600
*	# = 8	THEN BAUD =	1200
*	# = 9	THEN BAUD =	1800
*	# = :	THEN BAUD =	2400
*	# = ;	THEN BAUD =	3600
*	# = <	THEN BAUD =	4800
*	# = =	THEN BAUD =	7200
*	# = >	THEN BAUD =	9600
*	# = ?	THEN BAUD =	19.2K

THERE ARE FOUR SHIFT CONTROL (EXT) FUNCTIONS

EXT O - OFFLINE MODE

EXT E - ONLINE TO ECLIPSE

EXT R - ONLINE TO RPU

EXT B - TRANSMIT BREAK TO ONLINE PORT

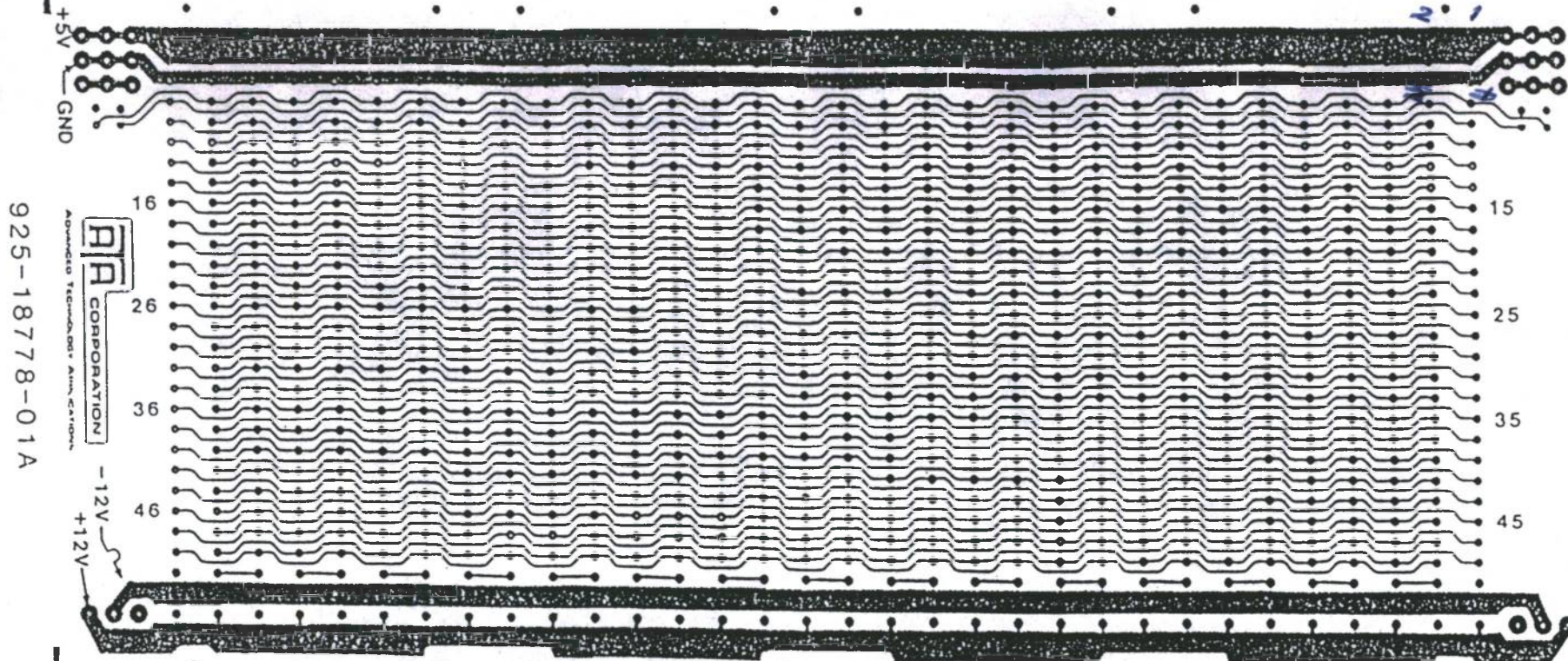
MEMORY MAP

<u>ADDRESS</u>	<u>LOCATION</u>	<u>COMMENT</u>
0000-03FF	6809 PCB	Ram-Zero Page, Stack, User
0800-0Bff	6809 PCB	Ram-User
9000-9003	ECL/RPU Interface	6551-Eclipse Communication Port
9004-9007	ECL/RPU Interface	6551-RPU "
9100-91FF	Control Panel Interface	9100-9101-CP Board 0
		9102-9103-CP Board 1
		9104-9105-CP Board 2
		9106-9107-CP Board 3
		9108-9109-CP Board 4
9820-982F	6809 PCB	6522-U22, Shaft Encoders
9840-984F	6809 PCB	6522-U19, Keyboard
9880-9883	6809 PCB	6551-U18, Debug Port
A000-ABFF	CRT Controller PCB	A000-A3FF Control Registers
		A400-ABFF Video Ram
C800-CFFF	ECL/RPU Interface	Ram-Save Video
E000-EFFF	6809 PCB	Rom 0-Control Panel Key Data
F000-FFFF	6809 PCB	Rom 1-Terminal Program

* these two blocks are not distinguished on 10805 card

BACK VIEW

components →



Control Panel Backplane
Standard Bus

	COMPONENT SIDE				CIRCUIT SIDE			
	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION
LOGIC POWER BUS	1	+5V	In	+5 Volts DC (Bussed)	2	-5V	In	-5 Volts DC (Bussed)
	3	GND	In	Digital Ground (Bussed)	4	GND	In	Digital Ground (Bussed)
	5	-5V	In	-5 Volts DC	6	-5V	In	-5 Volts DC
DATA BUS	7	D3	In/Out	Low Order Data Bus	8	D7	In/Out	High Order Data Bus
	9	D2	In/Out	Low Order Data Bus	10	D6	In/Out	High Order Data Bus
	11	D1	In/Out	Low Order Data Bus	12	D5	In/Out	High Order Data Bus
	13	D0	In/Out	Low Order Data Bus	14	D4	In/Out	High Order Data Bus
ADDRESS BUS	15	A7	Out	Low Order Address Bus	16	A15	Out	High Order Address Bus
	17	A6	Out	Low Order Address Bus	18	A14	Out	High Order Address Bus
	19	A5	Out	Low Order Address Bus	20	A13	Out	High Order Address Bus
	21	A4	Out	Low Order Address Bus	22	A12	Out	High Order Address Bus
	23	A3	Out	Low Order Address Bus	24	A11	Out	High Order Address Bus
	25	A2	Out	Low Order Address Bus	26	A10	Out	High Order Address Bus
	27	A1	Out	Low Order Address Bus	28	A9	Out	High Order Address Bus
	29	A0	Out	Low Order Address Bus	30	A8	Out	High Order Address Bus
CONTROL BUS	31	WR*	Out	Write to Memory or I/O	32	RD*	Out	Read to Memory or I/O
	33	IOR*	Out	I/O Address Select	34	MEMRO*	Out	Memory Address Select
	35	IOEXP*	In/Out	I/O Expansion	36	MEMEX*	In/Out	Memory Expansion
	37	REFRESH*	Out	Refresh Timing	38	MCSYNC*	Out	CPU Machine Cycle Sync.
	39	STATUS 1*	Out	CPU Status	40	STATUS 0*	Out	CPU Status
	41	BUSAK*	Out	Bus Acknowledge	42	BUSRO*	In	Bus Request
	43	INTAK*	Out	Interrupt Acknowledge	44	INTRO*	In	Interrupt Request
	45	WAITRO*	In	Wait Request	46	NMIRO*	In	Non-Maskable Interrupt
	47	SYSRESET*	Out	System Reset	48	PBRESET*	In	Push Button Reset
	49	CLOCK*	Out	Clock from Processor	50	CNTRL*	In	AUX Timing
POWER BUS	51	PCO	Out	Priority Chain Out	52	PCI	In	Priority Chain In
	53	AUXGND	In	AUX Ground (Bussed)	54	AUXGND	In	AUX Ground (Bussed)
	55	AUX+	In	AUX Positive (+12 Volts DC)	56	AUX-V	In	AUX Negative (-12 Volts DC)

7-14 Data
15-20 A5-67
A13 14 15

10804A 6502 STD CARD ADDRESS ROM

CUSTOMER } Joe Santistevan
 NAME & CO } Computer Image
 PO # 6551
 Rom # 4120

DATE 9/3/81

288 BIN #	288 HEX ADR	288 HEX DATA
14 AB15	ADE	00
13 AB14	ADD	01
12 AB13	ADC	02
11 AB12	ADB	03
10 AB11	ADA	04
9 N.C.	D08	05
8 RAM IC1	D07	06
7 RAM IC2	D06	07
6 RAM IC3	D05	08
5 RAM IC4	D04	09
4 INTIO	D03	0A
3 MEMIC	D02	0B
2 IORIC	D01	0C
1 ROM IC6		

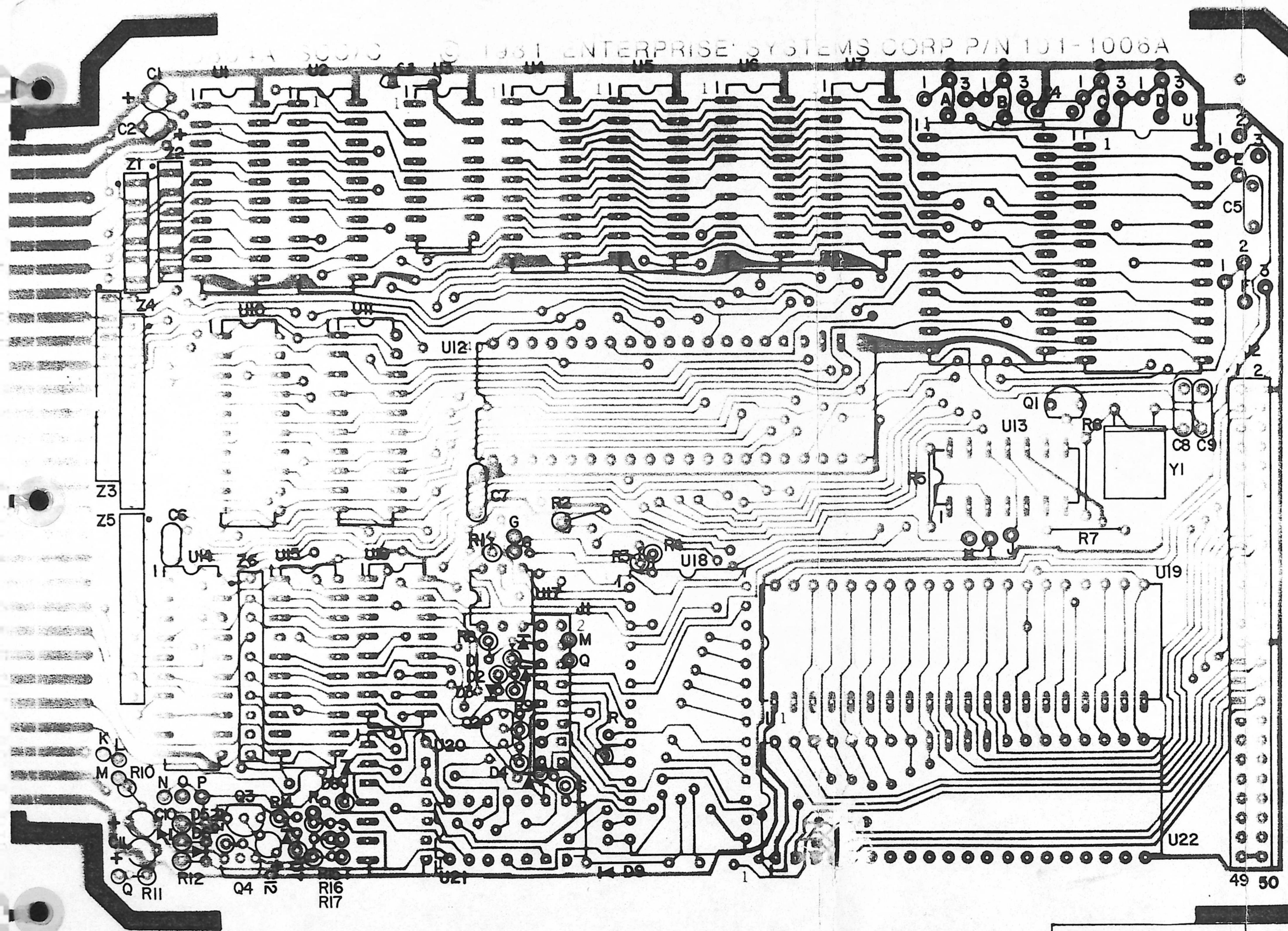
MEMORY ASSIGNMENT

0000	0 0 0 0 0	0 0 1 1	1 1 1 1	00	3F	RAM 0
0800	0 0 0 0 1	0 1 0 1	1 1 1 1	01	5F	RAM 1
1000	0 0 0 1 0	0 1 1 1	0 1 1 1	02	77	External Memory
1800	0 0 0 1 1			03	77	
2000	0 0 1 0 0			04	77	
2800	0 0 1 0 1			05	77	
3000	0 0 1 1 0			06	77	
3800	0 0 1 1 1			07	77	
4000	0 1 0 0 0			08	77	
4800	0 1 0 0 1			09	77	
5000	0 1 0 1 0			0A	77	
5800	0 1 0 1 1			0B	77	
6000	0 1 1 0 0			0C	77	
6800	0 1 1 0 1			0D	77	
7000	0 1 1 1 0			0E	77	
7800	0 1 1 1 1			0F	77	
8000	1 0 0 0 0			10	77	
8800	1 0 0 0 1	0 1 1 1	0 1 1 1	11	77	External Memory
9000	1 0 0 1 0	0 1 1 1	0 0 1 1	12	73	External I/O
9800	1 0 0 1 1	0 1 1 0	1 1 1 1	13	6F	Internal I/O
A000	1 0 1 0 0	0 1 1 1	0 1 1 1	14	77	External Memory
A800	1 0 1 0 1			15	77	
B000	1 0 1 1 0			16	77	
B800	1 0 1 1 1			17	77	
C000	1 1 0 0 0			18	77	
C800	1 1 0 0 1			19	77	
D000	1 1 0 1 0			1A	77	
D800	1 1 0 1 1	0 1 1 1	0 1 1 1	1B	77	External Memory
E000	1 1 1 0 0	0 1 1 1	1 1 1 0	1C	7E	ROM 0
E800	1 1 1 0 1	0 1 1 1	1 1 1 0	1D	7E	ROM 0
F000	1 1 1 1 0	0 1 1 1	1 1 0 1	1E	7D	ROM 1

6809 CHANGES

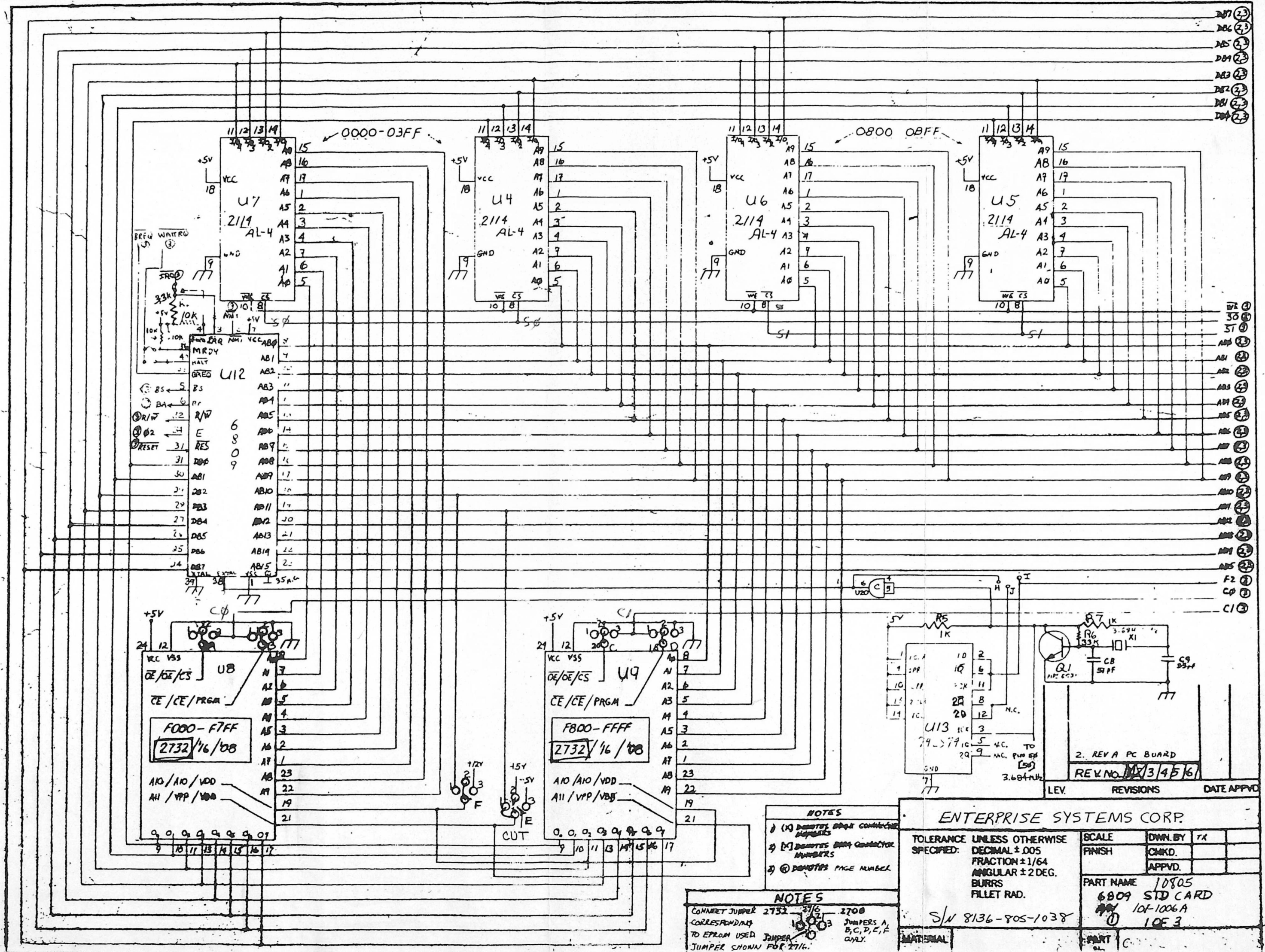
BLUE WIRE

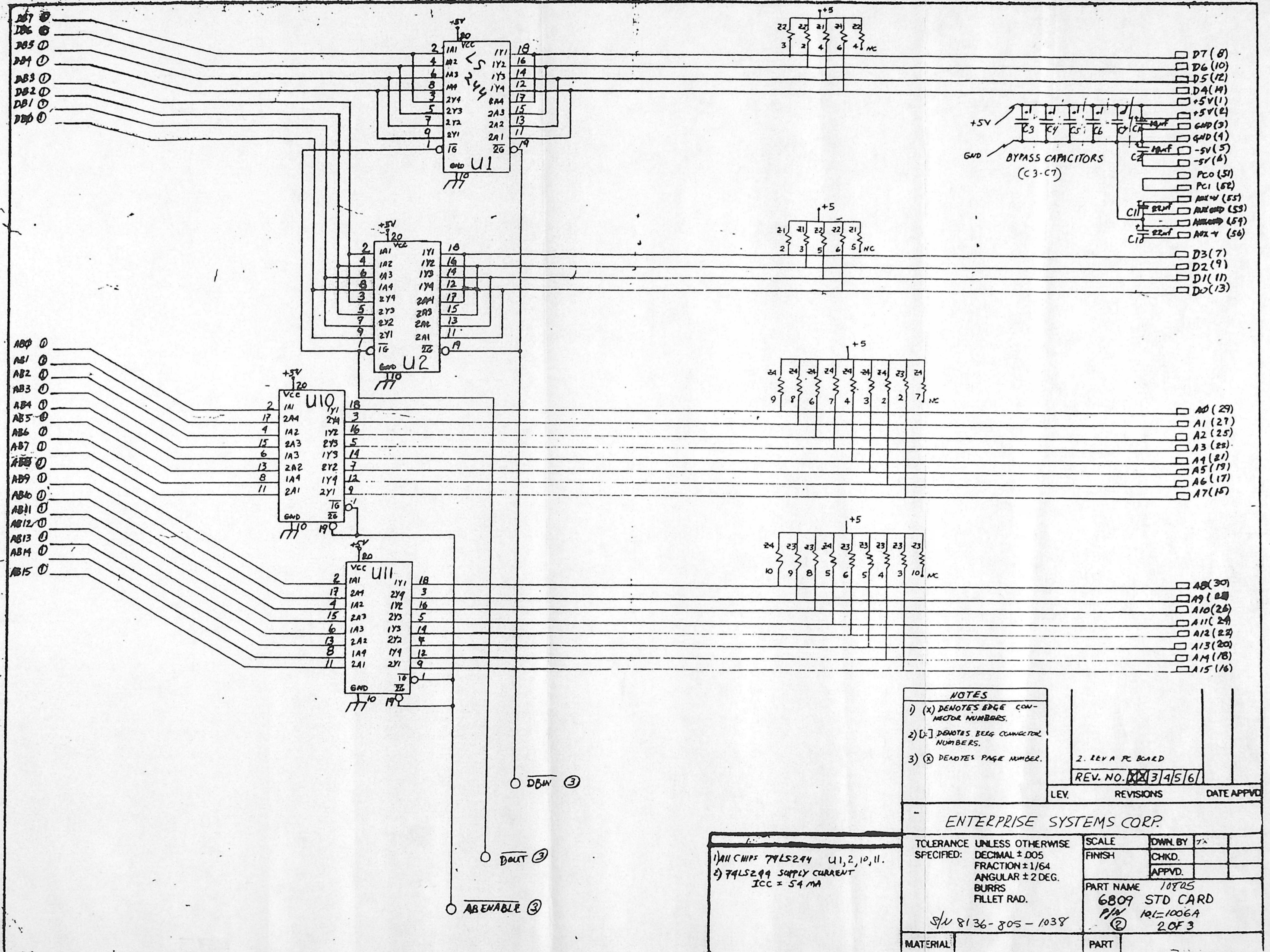
1. STRAP FOR 2732's
Locate jumper E
Cut etch from E to 2
Install jumper from E to 1
2. INSTALL UPPER RAM
Install 2114's into U5 & U6
3. GROUND DSR/ ON 6551 TO PREVENT SPURIOUS INTERRUPTS
Connect U18-17 to U18-16
4. PROVIDE CLOCK SIGNAL ON STANDARD BUS PIN 49
Add wire from U15-4 to U16-9
" " " U15-16 to Z5-4
" " " Z5-4 to STD Pin 49
5. PROVIDE 3.684 MHz CLOCK ON STANDARD BUS PIN 50
Add wire from U13-3 to STD Pin 50
6. PROVIDE NMI/ FROM 6551 TO 6809 FOR DEBUGGER
Cut etch from U15-5 to Z6-8
" " " U15-5 to U12-2
Add IN4148 diode from U15-5 to U12-2
Add wire from Z6-8 to U12-2
Isolate U18-26 from 3 IRQ/ etches at pin and reconnect 3 etches
Add wire from U18-26 to U12-2

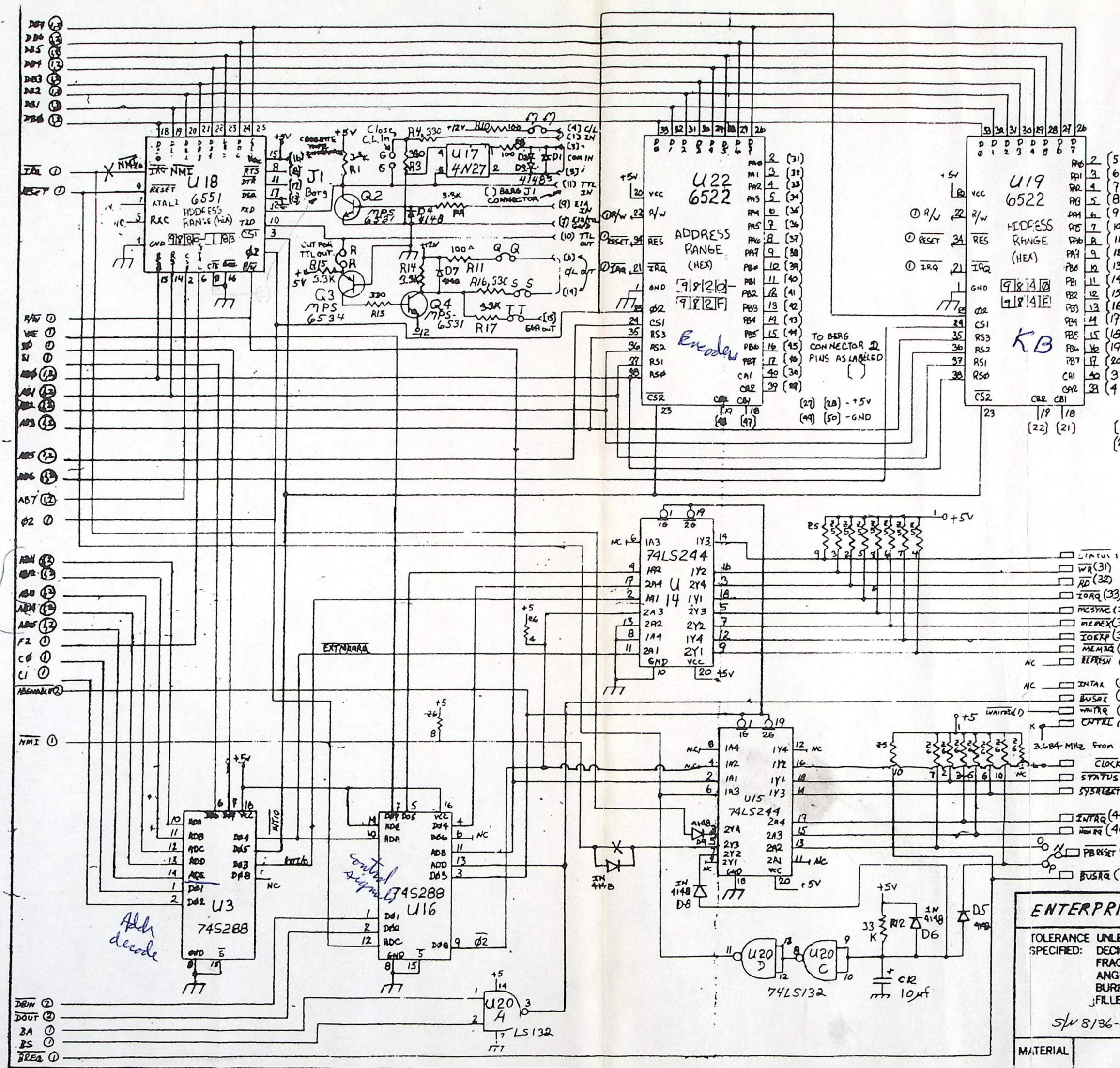


COMPONENT	VALUE
C1,2,10,11,12	10ufd/20v
C3,4,5,6,7	0.1 ufd
C8	51 pf
C9	33 pf
D1-9	1N4148
J1	16 pin jack
J2	50 pin jack
Q1,2,4	MPS6531
Q3	MPS6534
R1,2,9,14,15,17	3.3K, 1/4 w
R3,4,13,16	330 "
R5,7	1000 "
R6,12	33K "
R8,10,11	100 "
U1,2,10,11,14,15	74LS244
U3,16	74S288
U4,5,6,7	2114LC
U8,9	2708, 2716, or 2732
U12	6809
U13	74LS74
U17	4N27
U18	6551
U19,22	6522
U20	74LS132
Y1	3.6864 MHz
Z1,2	4.7K SIP, 6 pin
Z3,4,5,6	4.7K SIP, 10 pin

ENTERPRISE SYSTEMS CORP.
10805 6809 STD BUS SCC/C







TO BERG CONNECTOR 2
PINS AS LABELED []

{1}, {2} +5V
{23}, {24} GND

- ☐ STATUS (31)
- ☐ WR (31)
- ☐ RD (32)
- ☐ IRQ (33)
- ☐ MCSYNC (38) 02
- ☐ MEMEX (30)
- ☐ IOEXP (35)
- ☐ MEMREQ (34)
- ☐ REFRESH (37)
- ☐ NC
- ☐ INTAK (43)
- ☐ BUSAK (41)
- ☐ WAITR (45)
- ☐ CTRL (50)
- ☐ NC
- ☐ WAITR (45)
- ☐ 3.684 MHz from U13-3
- ☐ CLOCK (47)
- ☐ STATUS 0 (40) R/W
- ☐ SYSTEM (47)
- ☐ INTAK (44)
- ☐ WAITR (46)
- ☐ PBRST (49)
- ☐ BUSAK (42)

NOTES
1 (1) DENOTES EDGE CONNECTOR NUMBERS.
2 (X) DENOTES BERG CONNECTOR NUMBERS.
3 (X) DENOTES PAGE NUMBERS.

3. REV A PC BOARD
2. SELECT CHANGES IN STD
REV. NO. 121456
LEV. REVISIONS DATE APPROV

ENTERPRISE SYSTEMS CORP.	
TOLERANCE UNLESS OTHERWISE SPECIFIED: DECIMAL ±.005 FRACTION ±1/64 ANGULAR ±2 DEG. BURRS FILLET RAD.	SCALE FINISH DOWN BY CHKD. APPROV.
PART NAME 6809 STD CARD P/N 101-106A S/N 8/36-805-1038	PART No.

EMPTY
SECTION

* C.I. TERMINAL KEYBOARD DESCRIPTION

* 5/14/81 B. UNDERHILL

* 3/24/82 REVISED AND DELIVERED TO CI FOR TEST

* EACH ENTRY IN THE TABLE CONSISTS OF 1 LINE DESCRIBING
1 KEY. THE FORMAT IS:

* K NAME,INTTYPE,INTID,ID,MODULE,KS#,KS#

* EX: K NUMBER_SEC,257,4,7,2,1,13

* NAME: THE KEY NAME. NO SPACES MAY BE USED. WHERE A
SPACE IS WANTED, USE UNDERSCORE INSTEAD.

* INTTYPE: INTERNAL TYPE#, 256 THRU 265

* INTID: INTERNAL ID#, 0 THRU 999

* ID: SWITCH LAMP ID#, 1 THRU 254. IF THIS IS
77400Q, DO NOT ENTER THE LINE.

* MODULE: MODULE NO, 1 THRU 5

* KS#: SWITCH POSITION. THE 2 KS NUMBERS MAY BE
IN EITHER ORDER. KS NUMBERS ARE 1 THRU 16.

* THERE MUST BE NO SPACES IN THE LIST OF PARAMETERS

* FOLLOWING "K".

* THE LIST DOES NOT NEED TO BE IN ANY PARTICULAR ORDER.

* THE LIST MUST BE TERMINATED BY FCB \$FF

K MACR

FCB \4+\$80-1

MODULE

FCB \3

ID#

IFNC \1,0

FCB \1-256

TYPE, LESS 256

ENDC

IFC \1,0

FCB \$FF

ENDC

FDB \2

INTERNAL ID

FCB KS\5+KS\6

WORD#/BIT#

FCC '\0'

NAME

ENDM

OPT G,MEX

KS1 EQU 0 DEFINITIONS OF KS NUMBERS

KS2 EQU 1

KS3 EQU 2

KS4 EQU 3

KS5 EQU 4

KS6 EQU 5

KS7 EQU 6

KS8 EQU 7

KS9 EQU 70Q

KS10 EQU 60Q

KS11 EQU 00Q

KS12 EQU 40Q

KS13 EQU 10Q

KS14 EQU 20Q

KS15 EQU 30Q

KS16 EQU 50Q

KSX EQU 100Q

DUMMY

ORG \$E000

FDB KKREP

POINTER TO REPEAT-KEYS TABLE

KKTAB K ?,256,0,0,1,X,X

DUMMY ENTRY FOR ID#0

* FOR UNDEFINED KEYS

PAGE

* THE LIST STARTS HERE

K .ACT_PARAM,257,19,22,2,3,12
K .ADJUST_COLORS,257,303,64,3,6,14
K .ADJUST_SEC,257,8,11,2,5,13
K .AMP_1,260,400,119,4,4,14
K .AMP_2,260,401,120,4,5,14
K .AMP_3,260,402,121,4,6,14
K .AMP_4,260,403,122,4,7,14
K .AMP_5,260,404,123,4,8,14
K .AMP_6,260,405,124,4,8,9
K .ANIMATE,256,2,2,1,3,16
K .ART,257,116,43,1,4,13
K .AUTO_SEC,257,5,8,2,2,13
K .AUX_SIG_1,262,4,147,5,8,16
K .AUX_SIG_2,260,806,207,5,7,16
K .AUX_SIG_3,260,807,208,5,6,16
K .AUX_SIG_4,260,808,209,5,5,16
K .AUX_SIG_5,260,809,210,5,4,16
K .AUX_SIG_6,260,810,211,5,3,16
K .BLEND,257,200,58,3,5,14
K .BLUE,267,5,193,3,3,10
K .BLUE_1,258,3,71,5,8,10
K .BLUE_2,258,6,74,5,7,10
K .BLUE_3,258,9,77,5,6,10
K .BLUE_4,258,12,80,5,5,10
K .BLUE_5,258,15,83,5,4,10
K .BLUE_FG_AMP,260,707,144,4,1,14
K .CAM_A,267,1,189,3,4,11
K .CAM_AUX_1,267,7,195,3,4,10
K .CAM_AUX_2,267,8,196,3,4,16
K .CAM_B,267,2,190,3,4,14
K .CENTER_X,259,8,91,5,5,9
K .CENTER_Y,259,9,92,5,5,12
K .CENTER_Z,259,10,93,5,5,15
K .COMPAS,259,11,94,5,2,9
K .CONTROL,256,1,1,2,3,16
K .CREATE,257,2,5,2,1,15
K .DEACT_PARAM,257,18,21,2,4,12
K .DELETE_FAIR,257,115,42,1,1,15
K .DELETE_GROUP,257,21,24,2,2,10
K .DELETE_KF,257,103,30,1,3,9
K .DELETE_NODE,257,17,20,2,4,10
K .DELTA_PHASE_3,260,602,133,4,6,16
K .DELTA_PHASE_6,260,605,136,4,8,15
K .DELTA_PHASE_1,260,600,131,4,4,16
K .DELTA_PHASE_5,260,604,135,4,8,16
K .DELTA_PHASE_2,260,601,132,4,5,16
K .DELTA_PHASE_4,260,603,134,4,7,16
K .DEPTH,260,102,106,5,5,13
K .DEPTH_FG_AMP,260,702,139,4,2,16
K .DETACH_ENC,257,130,57,5,1,9
K .DIMEN,257,12,15,2,2,9
K .DISPLY_PHASE,257,127,54,1,3,13
K .DOWN,257,120,47,1,2,16
K .EX_BLANK,262,3,156,3,2,10
K .FETCH_KF,257,123,50,1,1,9
K .FG_1_XFG_2,265,3,177,3,4,12
K .FG_2_XFG_3,265,5,179,3,4,15
K .FG_1,265,1,175,3,3,13
K .FG_2,265,2,176,3,3,9

K .FG_3,265,4,178,3,3,12
K .FG_4,265,6,180,3,3,15
K .FG_5,265,7,181,3,4,13
K .FG_6,265,8,182,3,4,9
K .FINE_INC,257,129,56,5,1,15
K .FLIP,257,128,55,1,3,15
K .FORWARD,257,300,61,3,6,10
K .FREQ_1,260,300,113,4,4,11
K .FREQ_2,260,301,114,4,5,11
K .FREQ_3,260,302,115,4,6,11
K .FREQ_4,260,303,116,4,7,11
K .FREQ_5,260,304,117,4,8,11
K .FREQ_6,260,305,118,4,8,13
K .FS,257,107,34,1,2,12
K .GET,257,3,6,2,2,15
K .GREEN,267,4,192,3,3,14
K .GREEN_1,258,2,70,5,8,14
K .GREEN_2,258,5,73,5,7,14
K .GREEN_3,258,8,76,5,6,14
K .GREEN_4,258,11,79,5,5,14
K .GREEN_5,258,14,82,5,4,14
K .GREEN_FG_AMP,260,706,143,4,1,10
K .GROUP,257,20,23,2,1,10
K .HBLST,260,3,102,4,5,15
K .HBLST_FG_AMP,260,708,145,4,3,11
K .HBLW,260,4,103,4,4,15
K .HBLW_FG_AMP,260,709,146,4,3,14
K .HEIGHT,260,101,105,5,4,13
K .HI_FREQ_H_SNC,263,4,170,3,7,12
K .HI_FREQ_S_SNC,263,3,169,3,7,15
K .HOLD,257,109,36,1,5,12
K .HORIZ_FG_AMP,260,701,138,4,2,11
K .INCLNT,259,12,95,5,2,12
K .INSERT,257,117,44,1,2,15
K .INTENS,260,103,107,5,3,10
K .INTENS_FG_AMP,260,704,141,4,1,16
K .IN_RANGE,257,15,18,2,5,12
K .KEEP_IT,257,302,63,3,8,14
K .LEFT,257,121,48,1,4,16
K .LINEAR,257,108,35,1,4,12
K .LOAD_WFM,257,23,26,2,4,9
K .LOW_FREQ,263,1,167,3,7,13
K .LUM,267,6,194,3,3,16
K .MAGNIFY_SIZE,260,803,150,5,6,13
K .MAKE_KF,257,124,51,1,2,9
K .MANUAL_SEC,257,6,9,2,3,13
K .MASK1_RADIUS,260,204,112,4,6,13
K .MASK2_ANGLE,260,203,111,4,5,9
K .MASK2_RADIUS,260,202,110,4,5,13
K .MASK3_ANGLE,260,201,109,4,4,9
K .MASK3_RADIUS,260,200,108,4,4,13
K .MED_FREQ,263,2,168,3,7,9
K .MERGE,257,202,60,3,5,16
K .MOVE_ALL_KF,257,102,29,1,5,9
K .MOVE_KF,257,101,28,1,4,9
K .MOVE_PARAM,257,104,31,1,5,13
K .NAME_SCENE,257,14,17,2,2,12
K .NAME_SEC,257,13,16,2,1,12
K .NODE,257,16,19,2,3,10
K .NUMBER_SEC,257,4,7,2,1,13

K .OVLAP,261,1,153,3,2,11
K .PERSPT,260,805,152,5,7,15
K .PHASE_1,260,500,125,4,4,10
K .PHASE_2,260,501,126,4,5,10
K .PHASE_3,260,502,127,4,6,10
K .PHASE_4,260,503,128,4,7,10
K .PHASE_5,260,504,129,4,8,10
K .PHASE_6,260,505,130,4,8,12
K .PLAYBACK,256,4,4,3,7,11
K .PRINT,257,400,68,2,4,15
K .PROPRT_X,259,2,85,5,6,9
K .PROPRT_Y,259,3,86,5,6,12
K .PROPRT_Z,259,4,87,5,6,15
K .PS_LIN,257,114,41,1,5,10
K .PUSH,257,125,52,1,4,15
K .RED,267,3,191,3,3,11
K .RED_1,258,1,69,5,8,11
K .RED_2,258,4,72,5,7,11
K .RED_3,258,7,75,5,6,11
K .RED_4,258,10,78,5,5,11
K .RED_5,258,13,81,5,4,11
K .RED_FG_AMP,260,705,142,4,1,11
K .REMOTE,257,307,197,2,5,9
K .RENAME,257,11,14,2,3,15
K .RESET,257,306,67,3,7,14
K .REVERSE,257,301,62,3,8,10
K .RIGHT,257,122,49,1,5,16
K .ROTATE,259,13,96,5,2,15
K .R_FS,257,112,39,1,2,10
K .R_LIN,257,113,40,1,4,10
K .R_SF,257,111,38,1,3,10
K .R_SFS,257,110,37,1,1,10
K .SAVE,257,10,13,2,5,15
K .SCENE_EDIT,256,3,3,3,5,11
K .SEC_CAMERA,257,9,12,2,1,9
K .SEC_OVLAP,262,2,155,3,2,14
K .SELECT_NODE,257,118,45,1,2,13
K .SELECT_SCENE,257,100,27,1,1,13
K .SEL_BLUE_FG,262,307,164,3,1,10
K .SEL_DEPTH_FG,262,302,159,3,1,15
K .SEL_GREEN_FG,262,306,163,3,1,14
K .SEL_HBLST_FG,262,308,165,3,2,13
K .SEL_HBLW_FG,262,309,166,3,2,9
K .SEL_HORIZ_FG,262,301,158,3,1,13
K .SEL_INTENS_FG,262,304,161,3,1,16
K .SEL_RED_FG,262,305,162,3,1,11
K .SEL_VERT_FG,262,303,160,3,1,12
K .SEL_WIDTH_FG,262,300,157,3,1,9
K .SET_FG_1,266,1,183,3,5,13
K .SET_FG_2,266,2,184,3,5,9
K .SET_FG_3,266,3,185,3,5,12
K .SET_FG_4,266,4,186,3,5,15
K .SET_FG_5,266,5,187,3,6,13
K .SET_FG_6,266,6,188,3,6,9
K .SF,257,106,33,1,3,12
K .SFS,257,105,32,1,1,12
K .SIZE,259,1,84,5,2,13
K .SKEW-XY,259,5,88,5,3,12
K .SKEW_XZ,259,7,90,5,3,9
K .SKEW_ZX,259,6,89,5,3,15

K .SPECIAL_SEC,257,7,10,2,4,13
K .SPEC_BLANK,262,1,154,3,2,16
K .SPLICE,257,201,59,3,5,10
K .STEP,257,305,66,3,7,10
K .STOP,257,304,65,3,7,16
K .STUB2,0,0,198,2,5,10
K .STUB3,0,0,199,3,2,12
K .STUB4,0,0,200,3,2,15
K .STUB5,0,0,201,3,6,12
K .STUB6,0,0,202,3,6,15
K .STUB7,0,0,203,4,3,10
K .STUB8,0,0,204,4,3,16
K .STUB9,0,0,205,5,3,11
K .STUB10,0,0,206,5,3,14
K .TRNSLT_X,259,14,97,5,4,9
K .TRNSLT_Y,259,15,98,5,4,12
K .TRNSLT_Z,259,16,99,5,4,15
K .UP,257,119,46,1,1,16
K .VANISH_PT_X,260,801,148,5,7,9
K .VANISH_PT_Y,260,802,149,5,7,12
K .VANISH_SIZE,260,804,151,5,7,13
K .VBLST,260,1,100,4,5,12
K .VBLW,260,2,101,4,4,12
K .VERT_FG_AMP,260,703,140,4,2,10
K .VIDEO_RATE,257,22,25,2,3,9
K .WFM_1,264,1,171,3,8,13
K .WFM_2,264,2,172,3,8,9
K .WFM_3,264,3,173,3,8,12
K .WFM_4,264,4,174,3,8,15
K .WIDTH,260,100,104,5,3,13
K .WIDTH_FG_AMP,260,700,137,4,2,14
K .XCHNG,257,126,53,1,5,15

FCB \$FF END OF LIST

* TABLE OF REPEATING KEYS

* FOR EACH REPEATING KEY, PUT THE ID# IN THIS TABLE

* TERMINATE THE TABLE BY \$FF

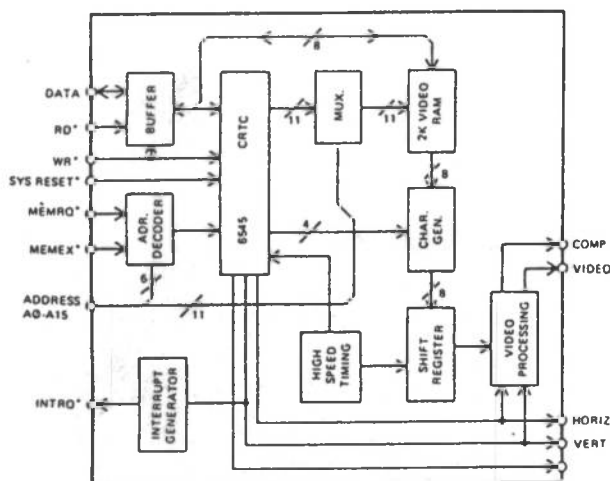
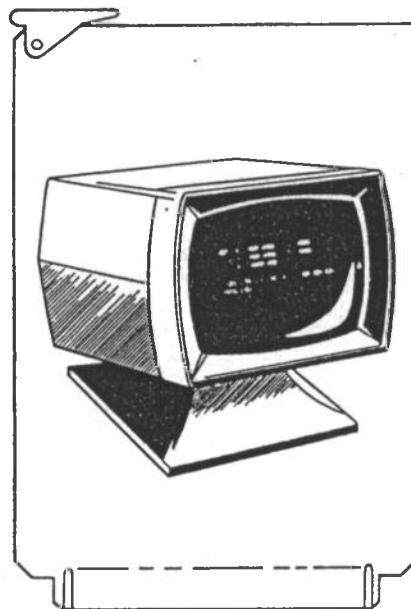
KKREP FCB 62 REVERSE
 FCB 61 FORWARD
 FCB \$FF
 END

FEATURES

- Fully programmable display and cursor format.
- Full alphanumeric and limited graphics.
- Full ASCII character set with descended lower case.
- 7 x 9 dot matrix characters.
- Inverse video and blink on a per-character basis.
- Programmable start address for scrolling.
- Up to 80 characters per line with standard horizontal sync.
- Interlace or non-interlace scan.
- External light pen capabilities.
- Single +5 volt supply.

APPLICATIONS

- CRT controller systems
- Data display terminals
- Point-of-entry systems
- Production control systems



The 97098 CRT Controller Card is designed to interface the STD Bus microprocessor families to CRT or TV-type raster scan displays. Display format, video timing and cursor control are fully bus programmable providing the user with a wide variety of display options.

Control of the circuit is achieved through the use of 18 data registers and one "pointer" (address) register. The data registers are loaded with constant parameters during system initialization, which determine horizontal and vertical timing, mode control, cursor attributes, start address and cursor location.

Video character data may be written to or read from the 2048-byte block of video refresh RAM. The host system can be interrupted on vertical retrace (if desired) to provide video RAM I/O without disturbing displayed information.

The card is memory mapped and occupies 3K bytes of memory.

INTERRUPT GENERATION

The user may select the interrupt feature by installing jumper No. J1. This interrupt is generated on every occurrence of the vertical sync pulse to signal the processor that the display is in retrace. It allows updating of the video RAM or CRTC without disturbing the video screen.

CHARACTER ACCENTS

Inverse video and blinking characters may be achieved on a per-character basis using the seventh or eighth data bit of video characters. Any one of four variations can be selected by proper placement of three jumpers.

① ② ③ ④
⑤ ⑥ ⑦ ⑧ Jumper Layout

- Upper case characters with software selectable character inverse and character blink. Jumper: 1 to 5, 2 to 6 and 3 to 4. The 97098 is shipped with this character accent selected. To alter this accent, cut the copper traces and install the necessary jumpers in step 2-4. The user selects character inverse by setting the eighth data bit of the character code to logical 1. Similarly, the character may be blinked by setting the seventh data bit of the character.

7th bit	8th bit	Accent
0	0	None
0	1	Character inverse
1	0	Character blink
1	1	Blinking inverse character

- Upper and lower case characters with software selectable character inverse. Jumper 1 to 2, 3 to 4 and 6 to 5.

The user selects character inverse by setting the eighth data bit of the character code to logical 1. Character blink is disabled.

- Upper and lower case characters with software selectable character blink. Jumper 1 to 2, 3 to 7, and 4 to 8.

The user selects character blink by setting the eighth bit of the character code to logical 1. Character inverse is disabled.

- Upper and lower case characters with software selectable character inverse-blink. Jumper 1 to 2, 4 to 3 and 7 to 3.

In this configuration, setting the eight data bit of the character code makes the character inversed and blinking.

CRTC REGISTER DESCRIPTION

Generation of video signals is controlled by the 6845 CRTC chip. The chip has 18 internal registers, which may be programmed by the user to obtain the desired video signals.

Address Reg.				Reg.	Register file	Programmed	Unit	# of bits							
4	3	2	1	0	#			7	6	5	4	3	2	1	0
0	0	0	0	0	R0	Horizontal total	# char.	V							
0	0	0	0	1	R1	Horizontal displayed	# char.	V							
0	0	0	1	0	R2	Horiz. sync position	# char.	V							
0	0	0	1	1	R3	Horiz. sync width	# char.	V	X	X	X	X	X	X	X
0	0	1	0	0	R4	Vertical total	# rows	V							
0	0	1	0	1	R5	Vert. total adjust	# scans	V	X	X	X	X	X	X	X
0	0	1	1	0	R6	Vertical displayed	# rows	V							
0	0	1	1	1	R7	Vert. sync position	# rows	V							
0	1	0	0	0	R8	Interlace mode	-	V	X	X	X	X	X	X	X
0	1	0	0	1	R9	Max scan line adr.	scanline	V	X	X	X	X	X	X	X
0	1	0	1	0	R10	Cursor start	scanline	V	X	X	X	X	X	X	X
0	1	0	1	1	R11	Cursor end	scanline	V	X	X	X	X	X	X	X
0	1	1	0	0	R12	Start address (H)	-	V	X	X					
0	1	1	0	1	R13	Start address (L)	-	V	X	X					
0	1	1	1	0	R14	Cursor location (H)	-	X/V	X	X					
0	1	1	1	1	R15	Cursor location (L)	-	X/V	X	X					
1	0	0	0	0	R16	Light pen (H)	-	X	X	X					
1	0	0	0	1	R17	Light pen (L)	-	X	X	X					

Address Register: This 5 bit write-only register is used as a pointer to any one of the 18 data registers. When accessing a data register, the 5-bit register address is first written to the address register (even card address), then the desired data is written to (or read from) the data register (odd card address).

Horizontal Total Register (R0): This 8 bit write-only register determines the horizontal sync frequency generated by the CRTC.

Horizontal Displayed Register (R1): This 8 bit write only register determines the number of displayed characters per horizontal line.

Horizontal Sync Position (R2): This 8 bit write only register determines the position of the horizontal sync pulse on a scan line.

Horizontal Sync Width (R3): This 4 bit write-only register determines the width of the horizontal sync pulse.

Vertical Total (R4) and Vert. Total Adjust (R5) registers: These registers are used together to determine the frequency of the vertical sync signal. To get an exact 50 or 60 Hz frequency R4 is loaded with the integer number of character row times closest to (but less than) that needed for the desired frequency, then R5 is loaded with the number of scan lines necessary to make the frequency exact.

Vertical Displayed Register (R6): This 7 bit write-only register determines the number of character rows displayed on the screen.

Vertical Sync Position (R7): This 7 bit write-only register determines the position of the vertical sync pulse.

Interlace Mode Register (R8): This 2 bit write-only register selects non-interlace scan, interlace sync scan or interlace sync and video scan.

Maximum Scan Line Address Register (R9): This 5 bit write-only register determines the number of scan lines per character row.

Cursor Start Register (R10): This 7 bit write-only register determines the first scan line of the cursor. In addition, two bits are used to specify cursor blink and the blink period.

Cursor End Register (R11): This 5 bit write-only register determines the last scan line of the cursor.

Start Address Registers (R12 and R13): These registers form a single 14 bit write-only register, which determines the first RAM address displayed on the screen. R12 is the high order bits and R13 is the low order byte. These registers can be used to implement hardware scrolling.

Cursor Registers (R14 and R15): These registers determine the location of the cursor on the screen. These are read/write registers with the high order bits in R14 and the low order byte in R15.

Light Pen Register (R16 and R17): These 14 bit read-only registers store the current refresh address when the light pen input pulses high.

Note: The 97098 CRT Controller Card does not include light pen capture circuitry. The address and data registers of the CRTC occupy a 1 k block of memory space. The address register is accessed as any even address of the 1 k block and is used as a "pointer" to any one of the 18 data registers. Data registers are accessed as any odd address of the 1 k block.

TOP-OF-CARD SIGNALS

The following signals are available through a standard, 9 pin D-type connector:

PIN 1. Composite video: 75 ohm impedance
PIN 2. Video: TTL compatible
PIN 3. Vertical sync: TTL compatible

PIN 4. Horizontal sync: TTL compatible
PIN 5. Light pen input: TTL compatible
PIN 6-9. Ground

Specifications

CRT Controller Card 97098

BOSS LINE

DIMENSIONS

- Meets STD Bus specifications
- 4.5 in. high by 6.5 in. long
- 0.5 in. maximum profile thickness

CARD INCLUDES

- 15 Mhz crystal dot rate clock
- 2K bytes slaved video RAM
- Vertical sync interrupt generation selectable by user.
- Jumper-selectable address decoding
- Jumper-selectable character accents
- 6845 CRT controller chip

BUS INTERFACE

- All signals meet STD Bus electrical specifications
- Card is memory-mapped and occupies 3K bytes of memory

EXTERNAL CONNECTIONS

- DE-9S connector provides composite video and separate video signals. (Cinch #DE-9S or equivalent). Mating connector 97098-909.

POWER REQUIREMENTS

- Vcc - +5 VDC $\pm$ 5% at 1.5 amps. (max.)
- GND - 0.0 volts

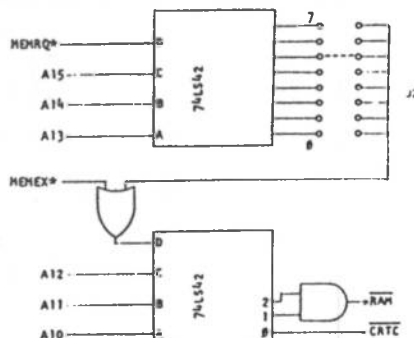
MEMORY MAPPING

The 97098 occupies a 3K byte block of memory space. Location of the block is user selectable for any of the following schemes:

Jumper	CRTC Registers	Video Ram
0	0000-03FF	0400-0BFF
1	2000-23FF	2400-2BFF
2	4000-43FF	4400-4BFF
3	6000-63FF	6400-6BFF
4	8000-83FF	8400-8BFF
5	A000-A3FF	A400-ABFF
6	C000-C3FF	C400-CBFF
7	E000-E3FF	E400-EBFF

ADDRESS JUMPER DEFINITION

The card is shipped with jumper no. 5 installed. The diagram below shows how the address decoding is accomplished.



CHARACTER DEFINITION

The following chart shows the codes for the character generator PROM. Note that these codes are the same as ASCII codes minus 20 (hex).

MSD

0	1	2	3	4	5	6	7
8	9	A	B	C	D	E	F
1	2	3	4	5	6	7	8
2	3	4	5	6	7	8	9
3	4	5	6	7	8	9	A
4	5	6	7	8	9	A	B
5	6	7	8	9	A	B	C
6	7	8	9	A	B	C	D
7	8	9	A	B	C	D	E
8	9	A	B	C	D	E	F
9	A	B	C	D	E	F	DEL
A	B	C	D	E	F	DEL	
B	C	D	E	F	DEL		
C	D	E	F	DEL			
D	E	F	DEL				
E	F	DEL					
F	DEL						

LSD

BOSS LINE EDGE CONNECTOR PIN LIST											
PIN NUMBER						PIN NUMBER					
OUTPUT (DRIVE)			OUTPUT (DRIVE)			INPUT (LOADING)			INPUT (LOADING)		
MNEMONIC			MNEMONIC			MNEMONIC			MNEMONIC		
+5 VOLTS	VCC	2	1	VCC	+5 VOLTS	GROUND	Gnd	3	GROUND	GROUND	
-5 VOLTS		6	5		-5 VOLTS						
D7	1	60	8	7	60	1	D3				
D6	1	60	10	9	60	1	D2				
D5	1	60	12	11	60	1	D1				
D4	1	60	14	13	60	1	D0				
A15	1		16	15		1	A7				
A14	1		18	17		1	A6				
A13	1		20	19		1	A5				
A12	1		22	21		1	A4				
A11	1		24	23		1	A3				
A10	1		26	25		1	A2				
A9	1		28	27		1	A1				
A8	1		30	29		2	A0				
RD*	1		32	31		1	WR*				
MEMRQ*	1		34	33			IORQ*				
MEMEX*	1		36	35			IOEXP*				
MCSYNC*			38	37			REFRESH*				
STATUS 0*			40	39			STATUS 1*				
BUSRQ*			42	41			BUSAK*				
INTRO*		60	44	43			INTAK*				
NMIRO			46	45			WAITRO*				
PBRESET*			48	47		1	SYSRESET*				
CNTRL*			50	49			CLOCK*				
PCI	IN		52	51	OUT		PCO				
AUX GND			54	53			AUX GND				
AUX -V			56	55			AUX +V				

*Designates Active Low Level Logic Eff. 01-01-80

Micro Link Corporation reserves the right to make changes any time in order to improve design and to supply the best product possible.

REPRESENTED BY:



INITIALIZING 97098 FOR 80 X 24 DISPLAY:

WRITE TO LOCATION A000 THE REG.# TO BE ACCESSED
WRITE TO LOCATION A001 THE CORRESPONDING VALUE.

REG.#	VALUE (HEX)
00	6C
01	50
02	58
03	09
04	1C
05	0D
06	10
07	16
08	00
09	08
0A	60
0B	0A
0C	00
0D	00
0E	00
0F	00

NOTE: THE VIDEO CONNECTOR PIN OUT HAS BEEN CHANGED FROM THE LISTING
IN THE DATA SHEET. THE NEW PIN ASSIGNMENTS ARE LISTED ON THE CORRECTION
SHEET (PART OF THE APPLICATION NOTE).

REF: 97098 CRT CONTROLLER CARD DATA SHEET

TOP-OF-CARD SIGNAL PIN-OUTS
(Incorrect)

CORRECT TOP-OF-CARD SIGNALS:

- PIN 1. Light pen input: TTL compatible
- PIN 2. Horizontal sync: TTL compatible
- PIN 3. Vertical sync: TTL compatible
- PIN 4. Video: TTL compatible
- PIN 5. Composite video: 75 ohm impedance

CRT Controller Card

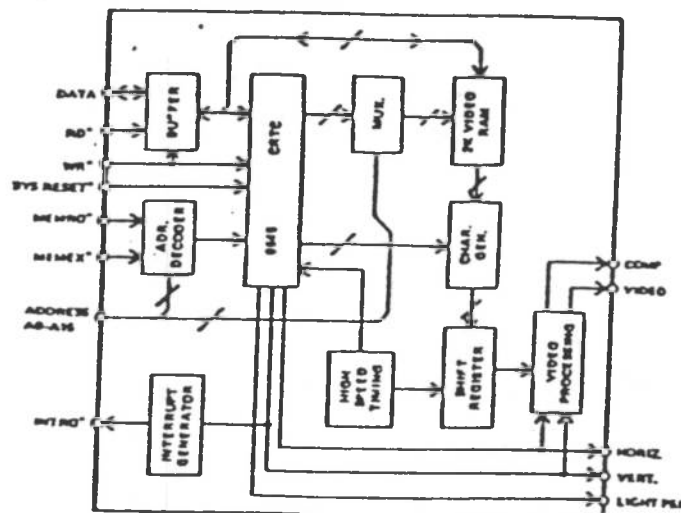
97098

APPLICATION NOTE: 97098 CRT CONTROLLER CARD

The 97098 CRT controller card is designed to interface the STD Bus microprocessor families to CRT or TV-type raster scan displays. This application note expands on the information found in the 97098 data sheet so the user may implement the card in a suitable host system.

DESCRIPTION OF THE CRT CONTROLLER

The primary function of the CRT controller card is to perform the raster-scan refresh of the video display. The card itself contains a Motorola 6845 CRT controller IC (or an equivalent), 2K bytes of slaved video refresh RAM, a 2716 EPROM character generator, video processing logic and bus interfacing.



6845 CRT Controller IC:

The 6845 CRTC consists of programmable horizontal and vertical timing generators, programmable linear address register, programmable cursor logic, light pen capture register, and control circuitry for bus interface. All CRTC timing is derived from the CRTC clock (T_c), the period of which is 0.6 microseconds. Comparators continuously compare counter contents to the contents of the programmable register file, $R_0 - R_{17}$ (See table 1).

For horizontal timing generation, comparisons result in a horizontal sync pulse of a frequency, position, and width determined by registers $R_0 - R_3$, and a horizontal display signal.

For vertical timing generation, comparisons result in a vertical sync pulse of a frequency and position determined by registers R4 - R7, and a vertical display signal. NOTE: The vertical sync pulse width is fixed at 16 raster lines in the vertical control section and is not programmable.

The linear address generator locates the relative positions of the character codes in video RAM with their positions on the screen. At the beginning of a screen scan, the address generator uses the contents of the start Address registers (R12 and R13) to determine the location in video memory where display data starts. The host system can use the start address registers to achieve hardware scrolling through 16K characters.

The cursor logic determines the cursor location, size, and blinking rate on the screen. All are programmable using registers R10, R11, R14, and R15.

The light pen input going high causes the current contents of the address generator to be latched in the light pen registers, R16 and R17. The contents of the registers are subsequently read by the host processor. NOTE: The 97098 card does not provide light pen "capture" circuitry necessary to realize this function.

Video RAM:

2K bytes of slaved video RAM is located on the card at address A400 through ABFF (as shipped). The host system puts characters on the video screen by writing the proper character codes to the desired location in RAM. The CRTIC chip uses this data in conjunction with the character generator to output the proper dot patterns to the video display.

The CRTIC addresses this block of RAM as 0000 through 07FF during the video scan. If the start address registers are loaded with 0000, the first character displayed (upper left corner of screen) will be whatever character code the host system wrote to RAM at A400.

Character Generator:

The character generator is a programmed 2716 EPROM which contains the dot patterns of the complete ASCII character set plus some graphic patterns. Space is available in the EPROM for 16 additional character dot patterns which may be programmed by the user. For more information on this subject, contact the Engineering department at Micro-Link Corp.

Bus Interface:

The CRT controller card interfaces to the STD Bus and meets all electrical specifications thereof. Signals used are defined on the back page of the 97098 Data Sheet.

Video Processing Logic:

This circuitry provides the actual video signals to the CRT, including both a composite video signal and separate video, horizontal sync and video sync signals. These signals are brought off the card through a standard, 9-pin D-type connector.

CRT SCREEN FORMAT

The CRT Controller is programmed in scan line, character time and character row time units. Figures 2 and 3 show the relationship between these units and the video screen format.

CRTC REGISTER FILE DESCRIPTION

Nineteen registers in the CRTC chip may be accessed by means of the data bus. (See table 1)

Address Register:

The address register serves as a pointer to access the remaining 18 data registers. It is a 5 - bit write only register. When accessing a data register, the 5 - bit data register address is first written to the address register, then the desired data is written to (or read from) the data register. The card is shipped with the address register as any even address in the range A000 - A3FE. The data register is any odd address in the same range. The memory mapping may be changed as shown in the 97098 data sheet.

Horizontal Timing Registers: R0 - R3

Figure 2 shows the visible display area of a typical CRT monitor giving the point of reference for horizontal registers as the left most displayed character position. Horizontal registers are programmed in character time units (Tc) with respect to the reference.

Horizontal Total Register: R0

This 8 - bit write - only register determines the horizontal sync frequency. It is the total number of displayed plus non-displayed character time units minus 1. ($R0 = Nhc - 1$)

Horizontal Displayed Register: R1

This 8 - bit write-only register determines the number of displayed characters per horizontal line. ($R1 = Nhcd$)

Horizontal Sync Position: R2

This 8 - bit write-only register determines the horizontal sync position during the horizontal scan. ($R1 \leq R2 < R0$)

Horizontal Sync Width: R3

This 4 - bit write-only register determines the width of the horizontal sync pulse in character times.

Vertical Timing Registers: R4 - R9

The point of reference for vertical registers is the top character position displayed. Vertical registers are programmed in character row times or scan line times.

Vertical Total Register: R4

Vertical Total Adjust Register: R5

The vertical sync frequency is determined by both R4 and R5. The calculated number of character row times is usually an integer plus a fraction to get exactly a 50 or 60 Hz vertical refresh rate. The integer number of character row times minus one is programmed in the 7 - bit write-only Vertical Total register; the fraction is programmed in the 5 - bit write-only Vertical Total Adjust register as a number of scan line times.

Vertical Sync Position: R6

This 7 - bit write-only register determines the number of displayed character rows on the video screen and is programmed in character row times.

Vertical Sync Position: R7

This 7 - bit write-only register determines the vertical sync position with respect to the reference and is programmed in character row times.

Interlace Mode Register: R8

This 2 - bit write-only register controls the raster scan mode. See section on Display Modes for operation.

Maximum Scan Line Address Register: R9

This 5 - bit write-only register determines the number of scan lines per character row including spacing. The programmed value is a max. Address and is one less than the number of scan lines needed. For the 97098 card, a minimum of 10 scan lines are needed for upper case characters and 12 scan lines are needed for lower case characters.

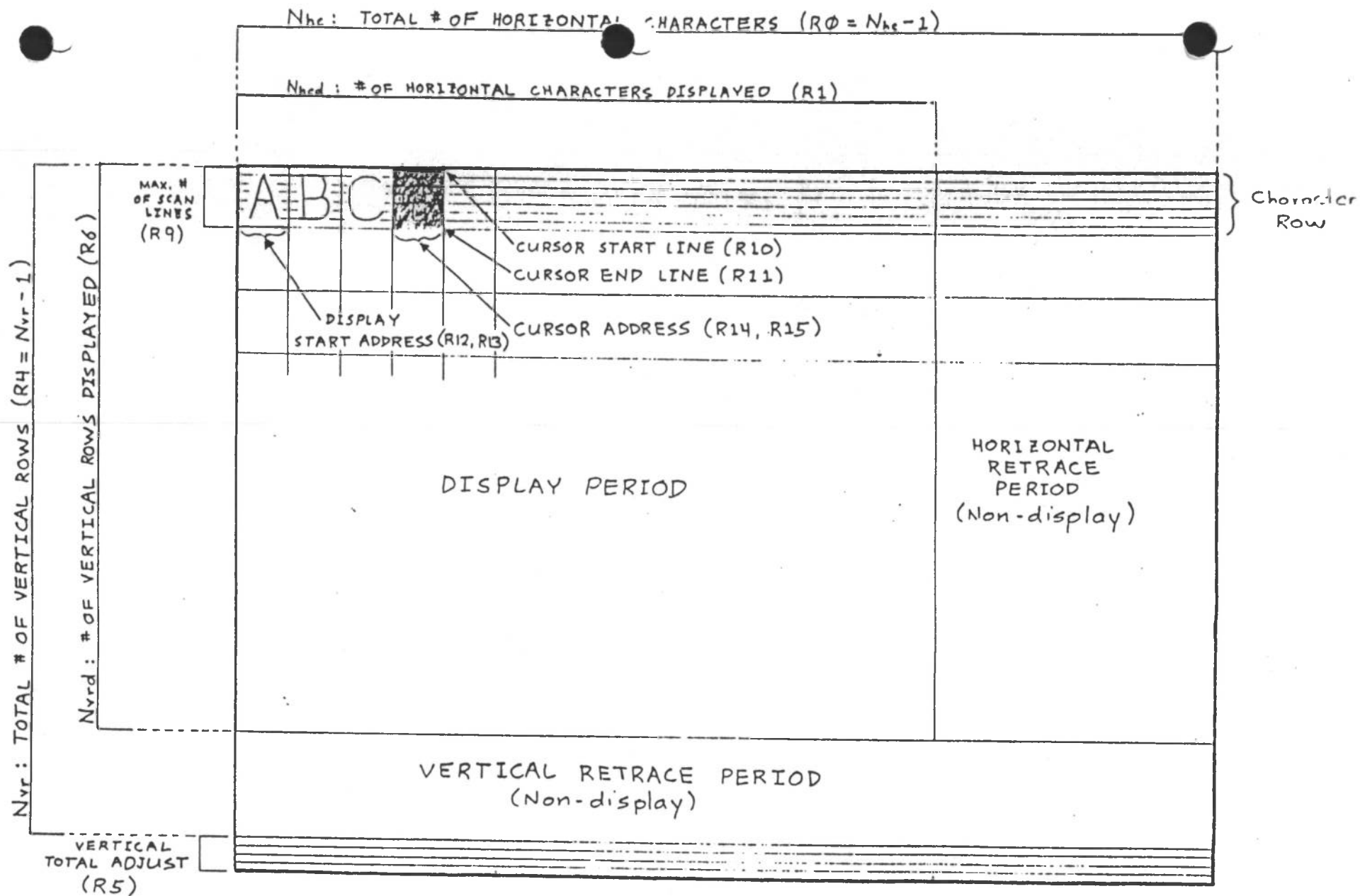
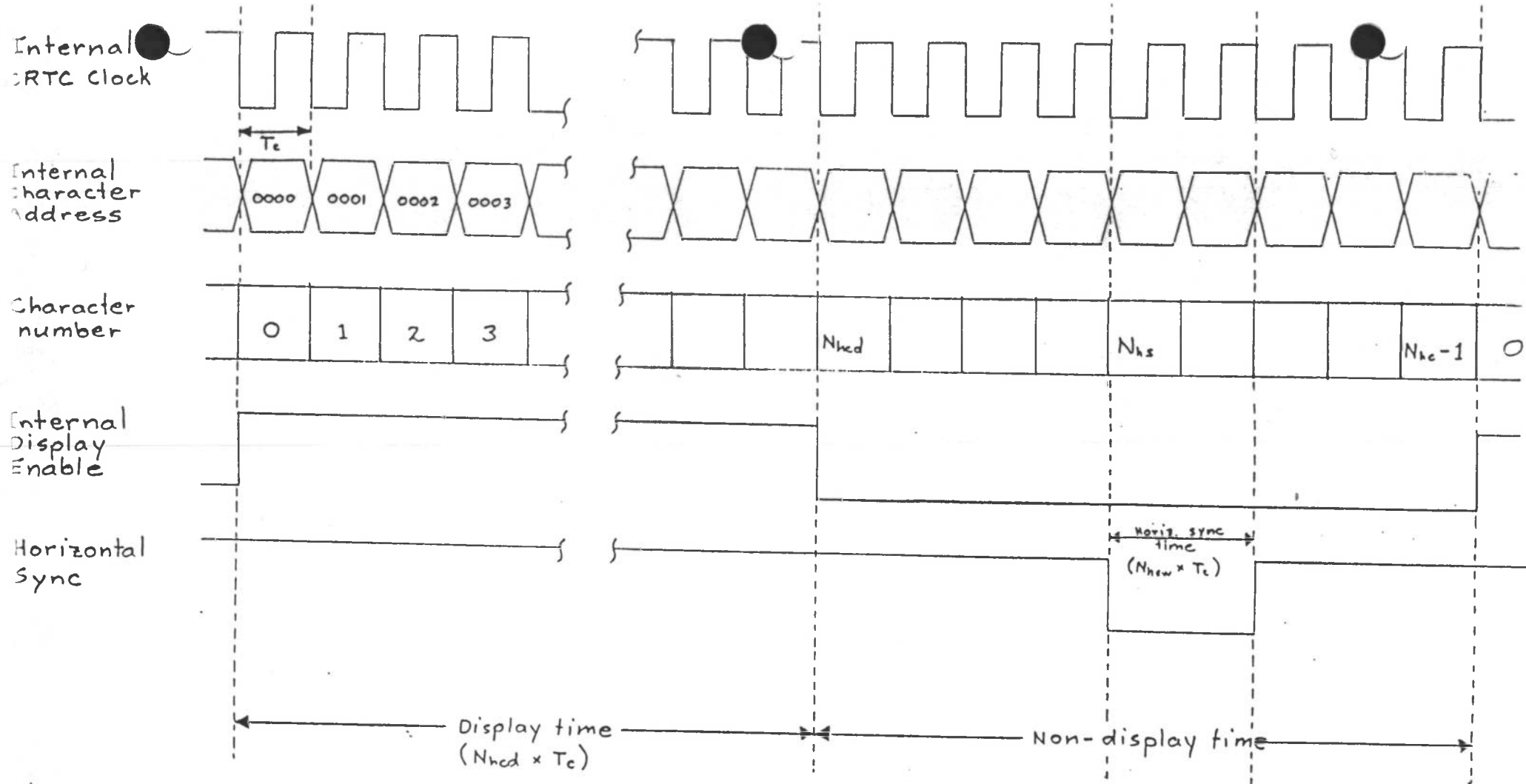


Figure 2 : CRT Screen Format



T_c = Internal CRTC clock period = $0.6 \mu s$ (15 MHz crystal)
 N_{hc} = Total number of horizontal character times (clock periods)
 N_{hcd} = Number of horizontal characters displayed
 N_{hs} = Position of horizontal sync in character times
 N_{hsw} = Horizontal sync width in character times

Figure 3 : Horizontal Scan Timing. This figure illustrates various horizontal timing parameters which are used to program the CRT controller registers. See section on registers R0 R1 R2 D2

Other Registers: R10 - R17

Cursor Start Register: R10

This 7 - bit write-only register controls the cursor format and the cursor start scan line. See section on Cursor Operation.

Cursor End Register: R11

This 5 - bit write-only register sets the cursor end scan line.

Start Address Registers: R12 and R13

These two registers form a 14 - bit read/write register which determines the first video RAM character address put out as a refresh address after vertical blanking. R12 is the 6 - bit high order register and R13 is the 8 - bit low order register.

Cursor Address Registers: R14 and R15

These two registers form a 14 - bit write-only register which determines the cursor location on the video screen. R14 is the 6 - bit high order register and R15 is the 8 - bit low order register.

Light Pen Address Registers: R16 and R17

These two registers form a 14 - bit read-only register which is used to store the contents of the address generator when the light pen input pulses high. R16 is the 6 - bit high order register and R17 is the 8 - bit low order register.

ADDRESS REGISTER					REGISTER #	REGISTER FILE	PROGRAM UNIT	READ	WRITE	# OF BITS							
4	3	2	1	0						7	6	5	4	3	2	1	0
X	X	X	X	X	X	ADDRESS REGISTER	-	NO	YES								
0	0	0	0	0	R0	Horizontal Total	char.	NO	YES								
0	0	0	0	1	R1	Horizontal Displayed	Char.	NO	YES								
0	0	0	1	0	R2	Horiz. Sync Position	Char.	NO	YES								
0	0	0	1	1	R3	Horiz. Sync Width	Char.	NO	YES								
0	0	1	0	0	R4	Vertical Total	Char. Row	NO	YES								
0	0	1	0	1	R5	Vert. Total Adjust	Scan Line	NO	YES								
0	0	1	1	0	R6	Vertical Displayed	Char. Row	NO	YES								
0	0	1	1	1	R7	Vert. Sync Position	Char. Row	NO	YES								
0	1	0	0	0	R8	Interlace Mode	-	NO	YES								
0	1	0	0	1	R9	Max. Scan Line Address	Scan Line	NO	YES								
0	1	0	1	0	R10	Cursor Start	Scan Line	NO	YES		B	P					
0	1	0	1	1	R11	Cursor End	Scan Line	NO	YES								
0	1	1	0	0	R12	Start Address (H)	-	NO	YES								
0	1	1	0	1	R13	Start Address (L)	-	NO	YES								
0	1	1	1	0	R14	Cursor Address (H)	-	YES	YES								
0	1	1	1	1	R15	Cursor Address (L)	-	YES	YES								
1	0	0	0	0	R16	Light Pen Adr. (H)	-	YES	NO								
1	0	0	0	1	R17	Light Pen Adr. (L)	-	YES	NO								

Table 1: CRTC Internal Register Assignment

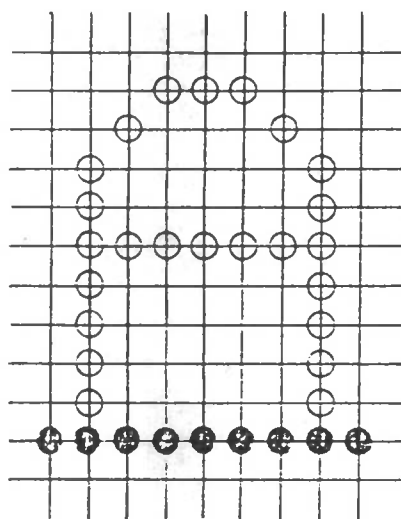
CURSOR OPERATION

The circuitry of the 97098 CRT controller card allows up to 16 scan lines per character row. Although the 6845 CRTC can be programmed for up to 32 lines, this is not compatible with the character generator setup.

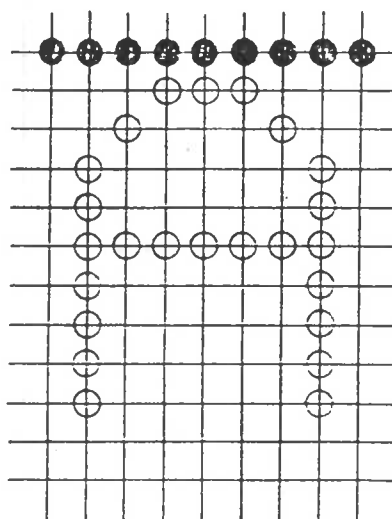
A one character wide cursor can be controlled by storing values into the cursor start (R10) and cursor end (R11) registers along with the cursor address registers (R14 and R15).

Bit 5 and bit 6 of the cursor start register (R10) control the cursor display and blink rate as follows:

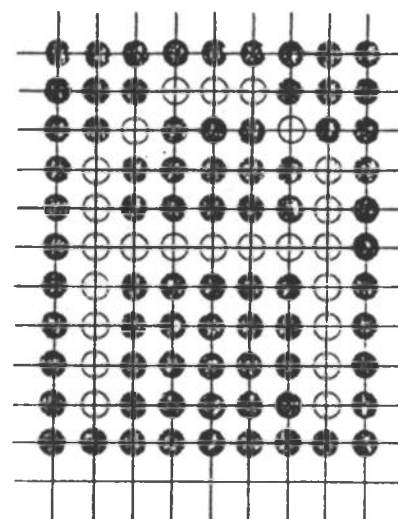
Bit 6	Bit 5	Cursor Operating Mode
0	0	Display cursor continuously
0	1	Blank cursor continuously
1	0	Blink cursor at 1/16 field rate
1	1	Blink cursor at 1/32 field rate



Under line Cursor
R10 = 0A, R11 = 0A



Overline Cursor
R10 = 00, R11 = 00



Block Cursor
R10 = 00, R11 = 0A

Figure 4 : Cursor Display Examples

A cursor of up to 16 scan lines in height can be displayed on and between the scan lines as loaded into R10 and R11. Some examples are shown in figure 4.

The cursor is positioned by changing the contents of the Cursor Address registers (R14 and R15). The cursor can be placed at any of the 16K character positions, thus facilitating hardware paging and scrolling through memory without loss of the cursor's original position.

DISPLAY MODES

An illustration of the three raster scan modes of operation is shown in figure 5.

Bit 1	Bit 0	Mode
0	0	Normal Sync Mode (Non-interlaced)
0	1	Interlace Sync Mode
1	1	Interlace Sync & Video Mode

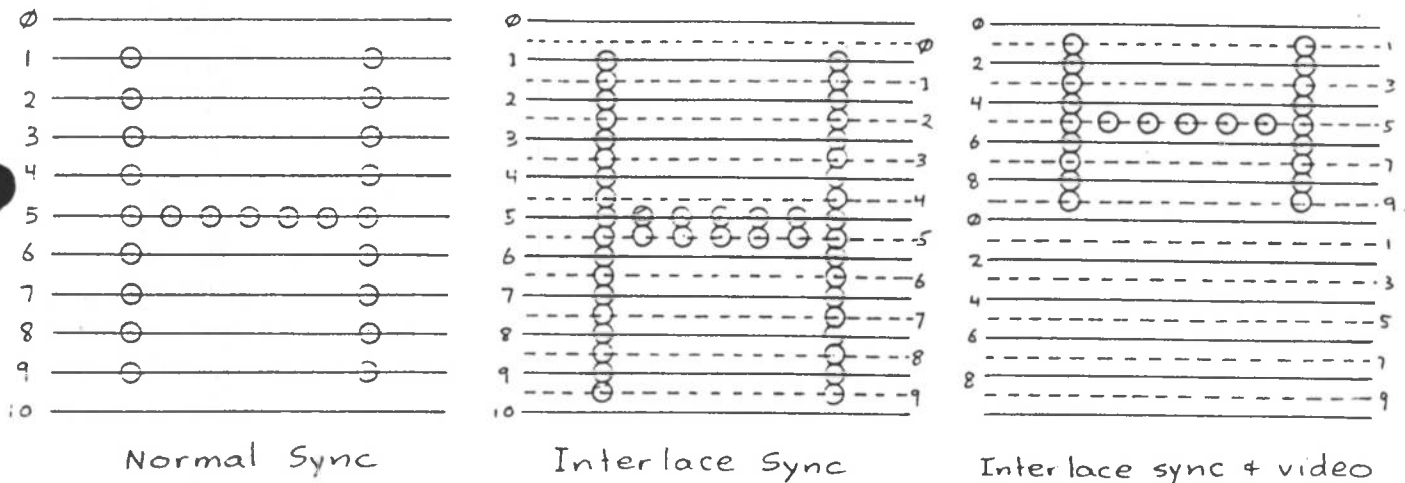


Figure 5: Interlace Control

Normal sync mode is non-interlaced. In this mode, each scan line is refreshed at the vertical field rate (e.g., 50 or 60 Hz). In the interlace modes, frame time is divided into even and odd alternating fields. The horizontal and vertical timing relationship results in the displacement of scan lines in the odd field with respect to the even field. When the same information is painted in both fields, the mode is called "Interlace Sync"; this is a useful mode for enhancing readability by filling in a character. When the even lines of a character are displayed in the even field and the odd lines in the odd field, the mode is called "Interlace Sync and Video." This last mode effectively doubles the character density on a monitor of a given bandwidth. The disadvantage of both interlace modes is an apparent flicker effect, which can be reduced by careful monitor design.

Some restrictions on interlace mode operation are:

- 1.) The total horizontal character count (Nhc) programmed into R0 must be odd in order to represent an even number of character-times for each horizontal scan.
- 2.) For Interlace Sync and Video mode only;
 - a.) The maximum scan line address (R9) must be odd (i.e., an even number of scan lines)
 - b.) The number of vertical rows displayed must be even. The programmed number in R6 must be one-half the actual number required.
 - c.) The cursor start and cursor end registers (R10 and R11) must both be even or both odd.

LIGHT PEN OPERATION

The Light Pen input of the 97098 CRT Controller is an active high signal which strobes the current contents of the CRTC address counter into the light pen registers, R16 and R17. The user must connect a suitable light pen capture circuit to this input which provides a pulse (min. width = 100ns) to the CRTC. NOTE: For normal CRTC operation, the light pen input is grounded by jumper J3. When using the light pen input, this jumper must be disconnected.

PROGRAMMING THE 97098 CRT CONTROLLER

Initialization:

The CRTC registers R0 - R15 must be initialized after power is applied to the system. The processor normally loads the timing parameters into the registers sequentially from a firmware table. The values in registers R0 - R11 are not changed after initialization in most systems. Table 2, figure 6 and figure 7 show some sample calculations and programming examples for 6800 and 8085 processor systems. Both software examples load the CRTC with timing parameters, clear the video screen, then stop. The addresses used in these examples are those of the card as it is shipped.

Scrolling:

The Start Address registers (R12 and R13) determine which memory location is the first displayed character on the screen. Since the CRTC linear address generator counts from this beginning count, the displayed portion of the screen may be a window on any continuous string of characters within a 16K block of refresh memory. In this manner, scrolling up or down is possible...by line, page or character.

Vertical Interrupt:

By installing jumper J1 on the circuit board, the user enables the vertical interrupt generated on every vertical sync pulse. This allows updating of video RAM and/or the CRTC registers during the vertical retrace non-display time, so that the displayed information is not disturbed.

Character Set and Accents:

Characters are displayed on the screen by writing the desired character codes to successive video RAM locations. The chart of figure 8 defines the character codes which must be written to the video RAM. Note that these codes are the same as ASCII codes minus 20 (hex), and that there are additional "graphic" characters provided for graphs, outlines or even games. Inverse video and blinking characters may be achieved on a per-character basis using the seventh or eighth data bit of the character codes. Any one of four variations can be selected by proper placement of three jumpers on the circuit board at location J4.

1	2	3	4	
0	0	0	0	
0	0	0	0	Jumper Layout, J4
5	6	7	8	

- Upper case characters with software selectable character inverse and character blink.
Jumper: 1 to 5, 2 to 6, and 3 to 4.

REG. #	REGISTER FILE	PROGRAM UNIT	CALCULATION *	PROGRAMMED VALUE	
				DECIMAL	HEX
R0	H TOTAL	Tc	$106 \times 0.6 = 63.6 \text{ US}$	$106-1=105$	69
R1	H DISPLAYED	Tc	$80 \times 0.6 = 48.0 \text{ US}$	80	50
R2	H SYNC POSITION	Tc	$86 \times 0.6 = 51.6 \text{ US}$	86	56
R3	H SYNC WIDTH	Tc	$6 \times 0.6 = 3.6 \text{ US}$	6	06
R4	V TOTAL	Tcr	$21 \times 763.2 = 16.03 \text{ MS}$	$21-1=20$	14
R5	V TOTAL ADJUST	Tsl	$11 \times 63.6 = 0.69 \text{ MS}$	11	0B
R6	V DISPLAYED	Tcr	$16 \times 763.2 = 12.21 \text{ MS}$	16	10
R7	V SYNC POSITION	Tcr	$17 \times 763.2 = 12.97 \text{ MS}$	17	11
R8	INTERLACE MODE	-		-	00
R9	MAX SCAN LINE ADR	Tsl		$12-1=11$	0B
R10	CURSOR START	Tsl	(SET FOR BLINK)	0	60
R11	CURSOR END	Tsl		$12-1=11$	0B
R12	START ADR (H)	-		0	00
R13	START ADR (L)	-		0	00
R14	CURSOR ADR (H)	-		0	00
R15	CURSOR ADR (L)	-		0	00

CRTC CLOCK PERIOD = Tc = 0.6 MS (with 15 MHz crystal)

SCAN LINE PERIOD = Tsl = Nhc X Tc = $106 \times 0.6 \text{ MS} = 63.6 \text{ MS}$

CHARACTER ROW PERIOD = Tcr = (# of scan lines) X Tsl = $12 \times 63.6 \text{ MS} = 736.2 \text{ MS}$

* These values are based on standard horizontal and vertical sync frequencies (15750 Hz horiz. sync, 60 Hz vert. sync) with the 97098's 15 MHz clock crystal.

TABLE 2: TYPICAL 80 X 16 SCREEN FORMAT INITIALIZATION OF THE 97098 CRT CONTROLLER.

0000	5F				CLR B	Clear Counter
0001	CE	00	20		LDX # \$ 20	Pointer to Table
0004	F7	A3	FE	CRTCIN	STA B \$A3FE	CRTC ADR. Register
0007	A6	00			LDA A 0,X	Get Table Data
0009	B7	A3	FF		STA A \$A3FF	Acc. to CRTC reg.
000C	08				INX	Increment Pointer
000D	5C				INC B	Increment Counter
000E	C1	10			CMP B \$ 10	Last CRTC reg.?
0010	26	F2			BNE CRTCIN	
0012	4F				CLR A	
0013	CE	A4	00		LDX # \$ A400	
0016	A7	00		CLEAR	STA A 0,X	Clear video screen
0018	08				INX	
0019	8C	AC	00		CPX # \$ AC00	
001C	26	F8			BNE CLEAR	
001E	20	FE		STOP	BRA STOP	Stop
0020	69	50	56	06		
0024	14	0B	10	11		
0028	00	0B	60	0B		
002C	00	00	00	00		

Figure 6: 97098 Initialization for 6800
Processor Systems

0000	AF				CLB	Clear Counter
0001	11	FF	A3		LPI DE, A3FFH	CRTC data reg.
0004	21	25	00		LPI HL, 0025H	Pointer to table
0007	32	FE	A3	CRTCIN	STAD A3FEH	
000A	46				LDB M	Get table data
000B	EB				XPDH	
000C	70				LDM B	Acc. to CRTC reg.
000D	EB				XPDH	
000E	23				INCP HL	Increment pointer
000F	3C				INC A	Increment counter
0010	FE	10			CPAI 10H	Last CRTC reg.?
0012	C2	07	00		JMP Z0, CRTCIN	
0015	06	00			LDBI 0	
0017	21	00	A4		LPI HL, A400H	
001A	70			CLEAR	LDM B	Clear video screen
001B	23				INCP HL	
001C	7C				LDA H	
001D	FE	AC			CPAI ACH	
001F	C2	1A	00		JMP Z0, CLEAR	
0022	C3	22	00	STOP	JMP STOP	Stop
0025	69	50	56	06		
0029	14	0B	10	11		
002D	00	0B	60	0B		
0031	00	00	00	00		

Figure 7: 97098 Initialization for 8085 Processor Systems

		Upper 4 bits							
		0	1	2	3	4	5	6	7
Lower 4 bits	0	SP	Ø	@	P	,	P		
	1	!	1	A	Q	a	q	—	
	2	"	2	B	R	b	r	┐	
	3	#	3	C	S	c	s	└	
	4	\$	4	D	T	d	t	┐	
	5	%	5	E	U	e	u	└	
	6	&	6	F	V	f	v	■	
	7	'	7	G	W	g	w		
	8	(	8	H	X	h	x	—	
	9	)	9	I	Y	i	y	┐	
	A	*	:	J	Z	j	z	└	
	B	+	;	K	[	k	{	┐	
	C	,	<	L	\	l		└	
	D	-	=	M	]	m	}	■	
	E	.	>	N	^	n	≈	■	
	F	/	?	O	_	o	DEL		

FIGURE 8: CHARACTER DEFINITION

The user selects character inverse by setting the eighth data bit of the character code to logical 1. Similarly, the character may be blinked by setting the seventh data bit of the character.

7th bit	8th bit	Accent
0	0	None
0	1	Character inverse
1	0	Character blink
1	1	Blinking inverse character

2. Upper and lower case character with software selectable character inverse.

Jumper: 1 to 2, 3 to 4, 5 to 6

The user selects character inverse by setting the eighth data bit of the character code to logical 1. Character blink is disabled.

3. Upper and lower case characters with software selectable character blink.

Jumper: 1 to 2, 3 to 7, 4 to 8.

The user selects character blink by setting the eighth bit of the character code to logical 1. Character inverse is disabled.

4. Upper and lower case characters with software selectable character inverse-blink.

Jumper: 1 to 2, 4 to 3, 7 to 3.

In this configuration, setting the eighth data bit of the character code makes the character inversed and blinking.

NOTE: The 97098 card is shipped with configuration #1

MEMORY MAPPING

The 97098 occupies a 3K byte block of the host systems memory space. Location of the block is user selectable with jumper J2 on the circuit board for any of the following address schemes:

Jumper #	CRTC Registers	Video RAM
0	0000 - 03FF	0400 - 0BFF
1	2000 - 23FF	2400 - 2BFF
2	4000 - 43FF	4400 - 4BFF
3	6000 - 63FF	6400 - 6BFF
4	8000 - 83FF	8400 - 8BFF
5	A000 - A3FF	A400 - ABFF
6	C000 - C3FF	C400 - CBFF
7	E000 - E3FF	E400 - EBFF

The 1K CRTC register block decodes the address and data register selection as follows:

- a. Any even address in the 1K block selects the CRTC address register.
- b. Any odd address in the 1K block selects the CRTC data registers.

TOP - OF - CARD SIGNALS

All video signals are accessed through a standard DE - 9S connector defined as follows:

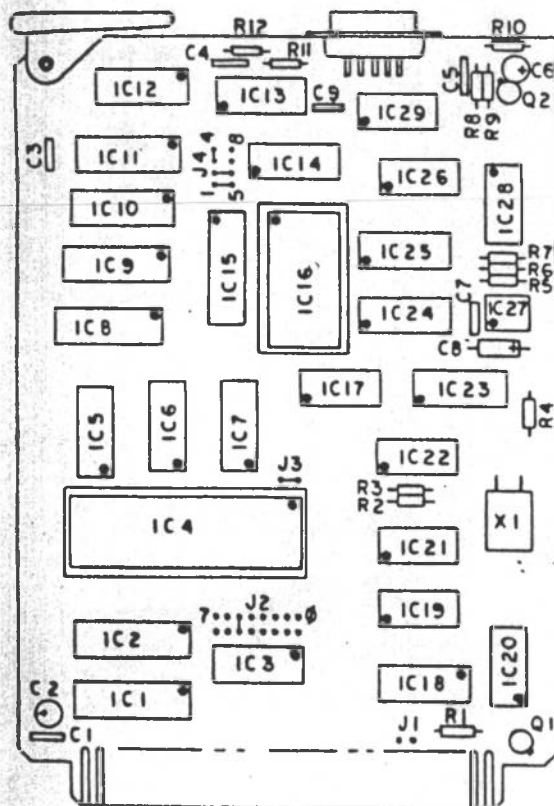
- Pin 1: Composite video signal, 75 OHM impedance. This signal contains the video dots, horizontal and vertical sync signals. It can be fed to a monitor or RF modulated and fed to a standard TV.
- Pin 2: Video signal, TTL compatible. This signal is the separate video dots without sync signals.
- Pin 3: Vertical sync signal, TTL compatible. This is a negative vertical sync output.
- Pin 4: Horizontal sync signal, TTL compatible. This is a negative horizontal sync output.
- Pin 5: Light pen input, TTL compatible. This is the light pen strobe input to the 6845 CRTC.
NOTE: Jumper J3 must be removed when using this input.

Pins 6 through 9 on the connector are tied to ground. If separate positive sync pulses are required for the monitor, a modification of the circuit board is required. This involves bypassing the inversion of the sync signals by a pair of NAND gates (IC 21). Refer to the circuit diagram or contact Micro-Link Corp. for further details.

Any questions or problems on the 97098 CRT Controller card may be directed to...

MICRO-LINK CORPORATION
624-B S. Range Line Rd.
Carmel, IN 46032

Telephone: (317) 846-1721
TWX: 810-260-2634



REF DES	QTY	DESCRIPTION	PART NO.	MANUF.	MICRO-LINK P.N.
C1,3	2	.1uf CAP.	C330C104M541CA	KEHMET	12250-104
C2,6	2	4.7uf CAP.	T390E475M050AS	KEHMET	12850-475
C4,7	2	.01uf CAP.	C062K103M2X5CA	KEHMET	1222C-103
C5	1	220PF CAP.	C312C21M2R5CA	KEHMET	12200-220
C8	1	10uf CAP.	T392C106K016AS	KEHMET	12450-106
C9	1	33PF CAP.			12200-330
IC1,2	2	OCTAL BUFFER	74LS244		52745-244
IC3,18	2	1 OF 10 DECODER	74LS42		52745-042
IC4	1	CRT CONTROLLER	6845		52230-845
IC5,6,7	3	QUAD DATA SEL	74LS157		52745-157
IC8-11	4	RAM 2114LV-3	2114		52130-114
IC12	1	QUAD D F/T	74174		52074-174
IC13	1	DUAL ONE SHOT	74123B+		52074-123
IC14	1	HEX/QUAD D F/T	74LS175		52745-175
IC15	1	8 BIT LATCH	74LS374B+		52745-374
IC16	1	2K X 8 EPROM	2716		52120-716
IC17	1	QUAD 2 INP OR	7432		52074-032
IC19,26	2	QUAD 2 INP OR	74LS32		52745-032
IC20,28	2	QUAD 2 INP AND	74LS08B+		52745-008
IC21	1	QUAD 2 INP NAND	74LS00		52745-000
IC22	1	HEX INVERTER	7404		52074-004
IC23	1	4 BIT COUNTER	74163		52074-163
IC24	1	SHIFT REGISTER	74165B+		52075-165
IC25	1	QUAD D F/T	74S175		52746-175
IC27	1	TIMER	555		52340-555
IC29	1	EXCLUSIVE OR	7486		52074-086
Q1	1	TRANSISTOR	2N2222		74311-222
Q2	1	TRANSISTOR	2N2369		74312-369
R1	1	4.7K, 1/4 W, 5% RES			72110-472
R2,3	2	680 OHM			72110-681
R4	1	2.7K			72110-272
R5	1	100K			72110-104
R6	1	27K			72110-273
R7	1	1.5K			72110-152
R8	1	68 OHM			72110-680
R9	1	220 OHM			72110-221
R10	1	10K			72110-102
R11	1	150 OHM			72110-151
R12	1	5.6K, 1/4 W, 5% RES			72110-562
X1	1	15 MHZ CRYSTAL	MP150	CRYSTAL	80140-150
	1	9 PIN CONN	DE9P	CINCH	28400-090
	1	40 PIN IC SOCKET	ICY-406-84G	R/N	28210-040
	1	24 PIN IC SOCKET	US2-24-110WB	SCANBE	28210-024
	1	CARD EJECTOR	610	SAE	38120-610
	1	PC BOARD			97098-701

MICRO-LINK		CRT CONTROLLER	
DES APP	7/7/84		
ISS NO.	1		
SCALE	1-1	ASSY	
SH. 1 OF 1		DWG NO. 97098-101	

PARTS

VECTOR BOARD 8x39 HOLES

2-.1 μ FARAD CAPS

3- 3M 3356 DUAL SOCKETS (14 POSITION)

1- 3M 3370 DUAL SOCKET (16 POSITION)

3- 3M 3397-1240 PLUG STRIP (24 CONTACT)

MAKE 6-7 CONTACT STRIPS 1240-7
2-8 CONTACT STRIPS 1240-8

1- 3M 3397-0240 SOLDER STRIP (24 CONTACT)

MAKE 4-4 CONTACT STRIPS 0240-4
2-3 CONTACT STRIPS 0240-3

2 FT- (APPROX) 26 GAUGE WIRE

1- 74LS04 -A1

1- 74LS08 -A2

1- 74LS74 -A3

1- 74LS85 -A4

SOLDER WIRE
TO SOLDER
STRIP CONTACTS
(22 PLACES)
LEAVE INSULATION
ON WIRE BETWEEN
STRIPS

SOLDER CAP
LEADS ONTO
1-CONTACT
STRIPS

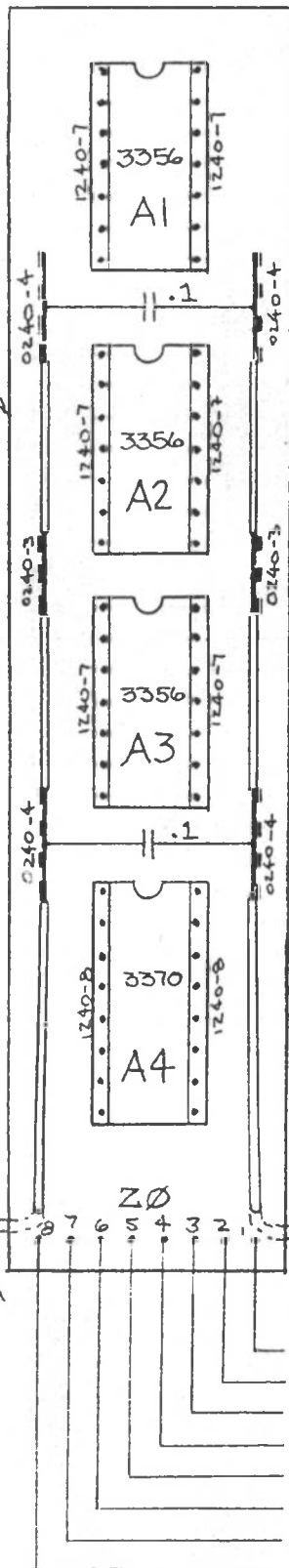
SOLDER TO
ROUND
WHERE IT
COMES IN FROM
BACKPLANE

SOLDER TO 15Y
WHERE IT COMES
IN FROM BACKPLANE

CBLNK TO IC17 PINS 12 & 13
RA3 FROM IC4-35
RA2 FROM IC4-36
RA1 FROM IC4-37
RA0 FROM IC4-38
VSYNCH FROM IC21-3
DISPEN FROM IC4-18
DISPEND TO IC12-3

RUN WIRE ON PCB FROM IC17-11 TO BACKPLANE PIN 37

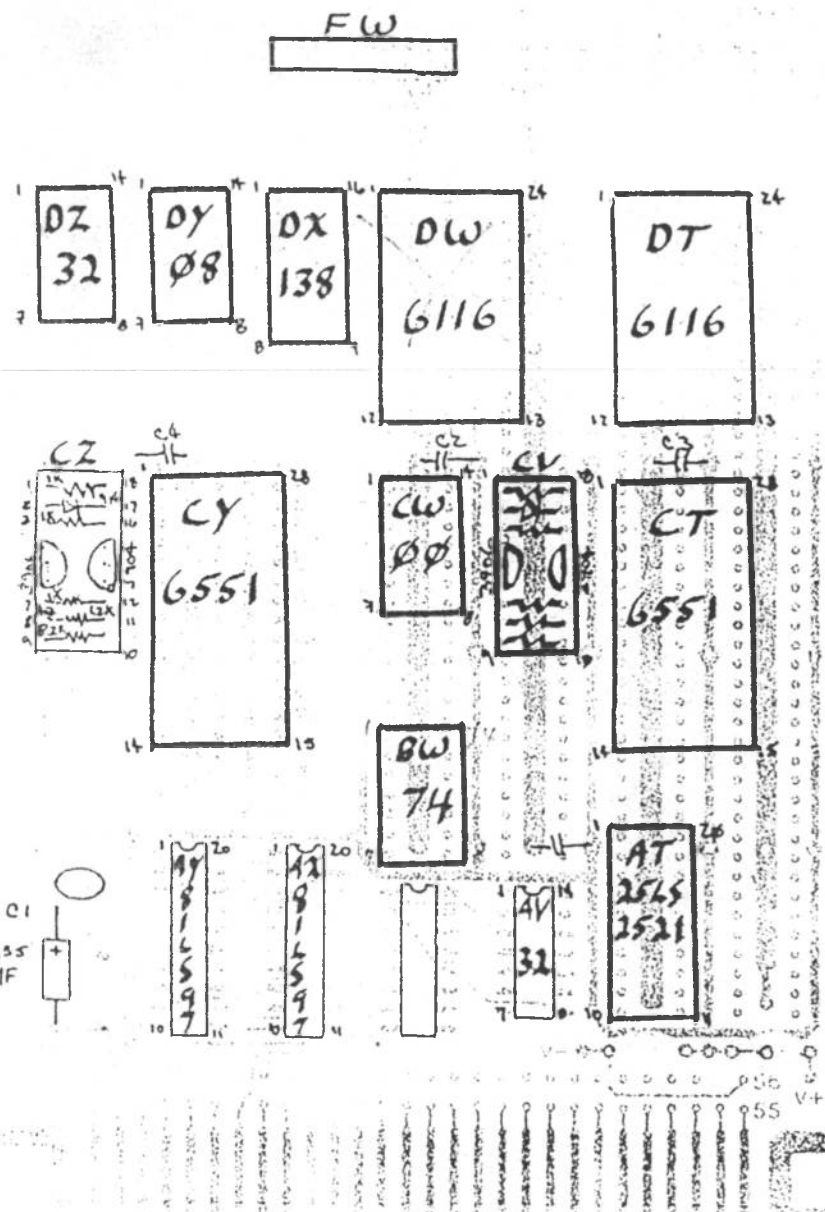
ATTACH THIS BOARD TO BACK OF CRT CONTROLLER
PCB WITH DOUBLE SIDED FOAM TAPE.



EMPTY
SECTION

MODIFICATIONS TO ATA SBWW1
FOR ECLIPSE/RPU-VIRTUAL VIDEO RAM

1. Cut etch AV-1 to bus pin 32 ($\overline{RD}$)
2. Cut etch AV-5 to bus pin 31 ($\overline{WR}$)
3. Cut etch AV-10 to bus pin 33 ($\overline{IORQ}$)



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

- 1 - 3M 20-PIN RIGHT ANGLE WIRE WRAP HEADER - FW
- 1 - 74LS00 CW
- 1 - 74LS08 DY
- 2 - 74LS32 AV, DZ
- 1 - 74LS138 DX
- 1 - 74LS74 BW
- 2 - H6116P-4 DT, DW HITACHI 200 nsec
- 1 - SY6551 CT, CY
- 1 - 81LS97 AX, AY
- 1 - 25LS2521 AT
- 1 - 1.35 MFD CAP C1
- 2 - ~~HEADER~~ ~~CY, CZ~~ WIX SOCKET 18 PIN
- 2 - 3904 MOTOROLA TRANSISTOR 13, 14, 15
- 2 - 3906 " " 4, 5, 6
- 2 - 9A DIODES 2
- 6 - 1K Ω 1/4 WATT RESISTORS 13, 7
- 2 - 1.2K Ω " " 8
- 2 - 8.2 Ω " " 9
- 4 - 1M CAPS C2, C3, C4, C5

TOLERANCES UNLESS
OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES
± ± ±

APPROVALS DATE

DRAWN DW 9/2/81

CHECKED

ATA CORP
COMPUTER IMAGE
CONTROL PANEL SYSTEM II

ELLIPSE/RPU-VIDEO RAM STD BUS

SCALE SIZE DRAWING NO.

11X15DI

DO NOT SCALE DRAWING

SHEET 1 OF 1

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

20 PIN
CONNECTOR
3M 3428

A

26 PIN
CONNECTOR
3M 3429

B

C
50 PIN CONNECTOR
3M 3433

+ OUT
1

+ IN
4

RELIABILITY, INC.

DC-DC CONVERTER

COM
2

10W5R12-12

3
- OUT

5
- IN

D

TOLERANCES UNLESS
OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES
± ± ±

APPROVALS

DATE

DRAWN

DW

9/7/81

CHECKED

ATA CORP
COMPUTER IMAGE
CONTROL PANEL SYSTEM IV
INTERCONNECT BOARD

SCALE

SIZE

DRAWING NO.

DO NOT SCALE DRAWING

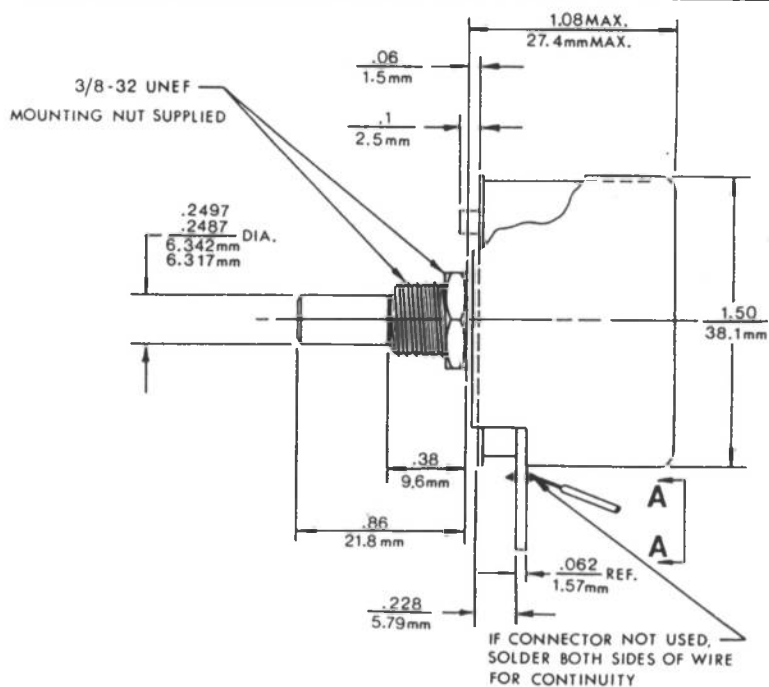
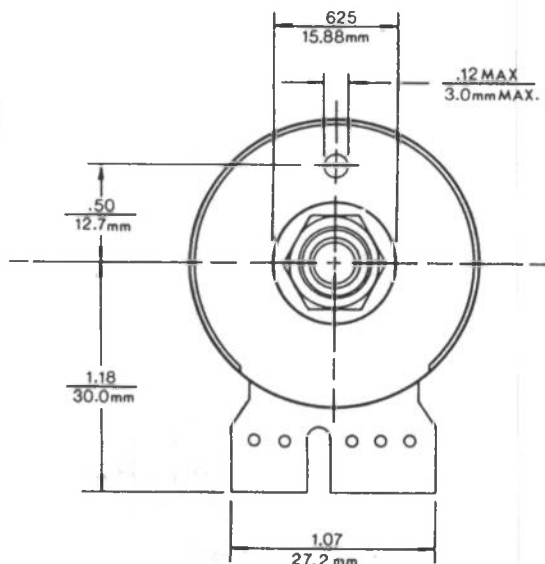
SHEET 1 of 1

PANELCODER™ SERIES

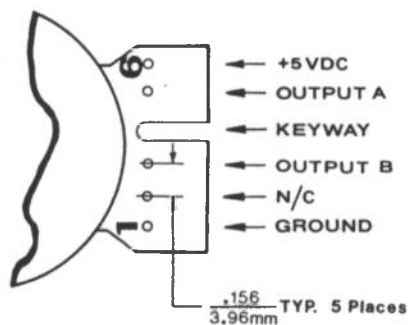
If you are considering eliminating old style potentiometers with their wiper wear and noise, the PANELCODER Series offers you the way to go digital economically. For further information, please contact our application Engineering Department.



PHYSICAL CHARACTERISTICS

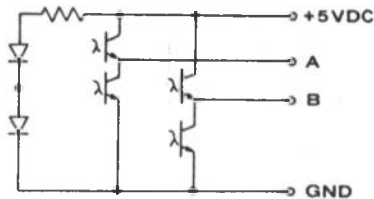
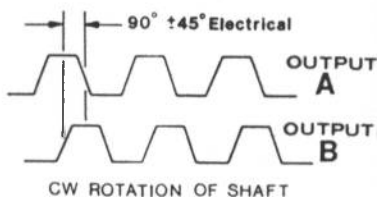


OUTPUT CONFIGURATIONS



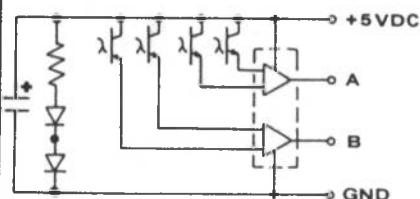
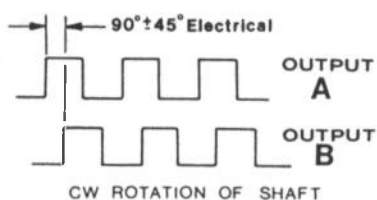
TERMINAL IDENTIFICATION
VIEW A-A

MODEL 66D



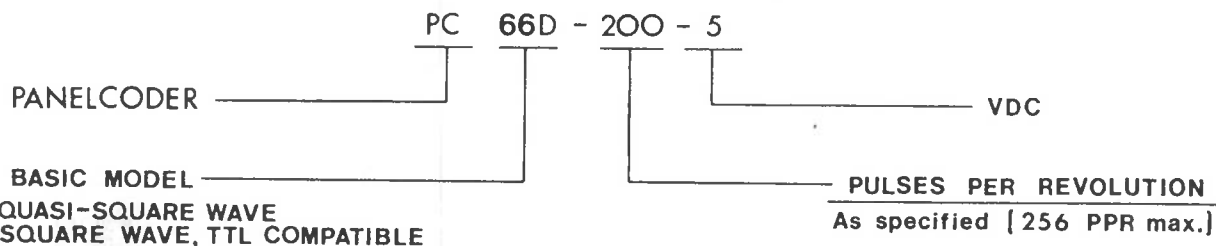
SCHEMATIC

MODEL 62D



SCHEMATIC

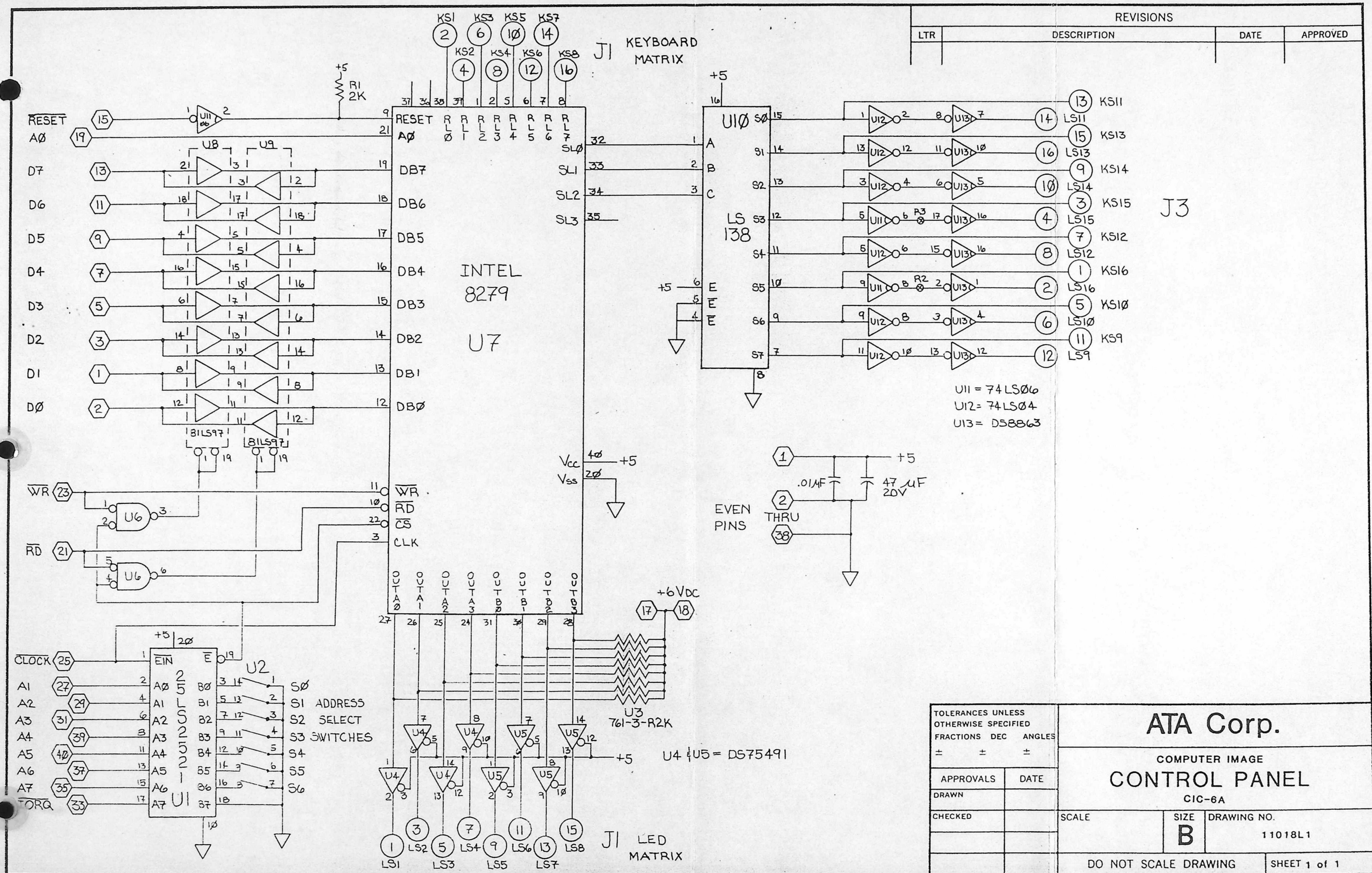
MODEL DESIGNATION



ORDERING INFORMATION

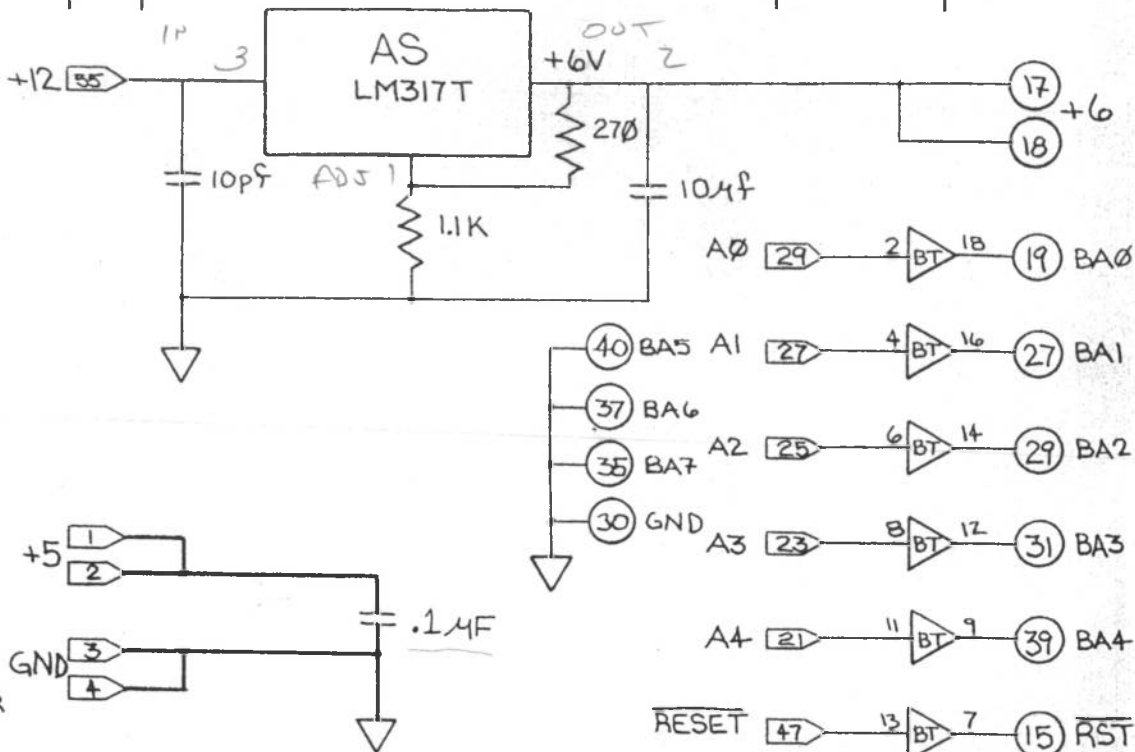
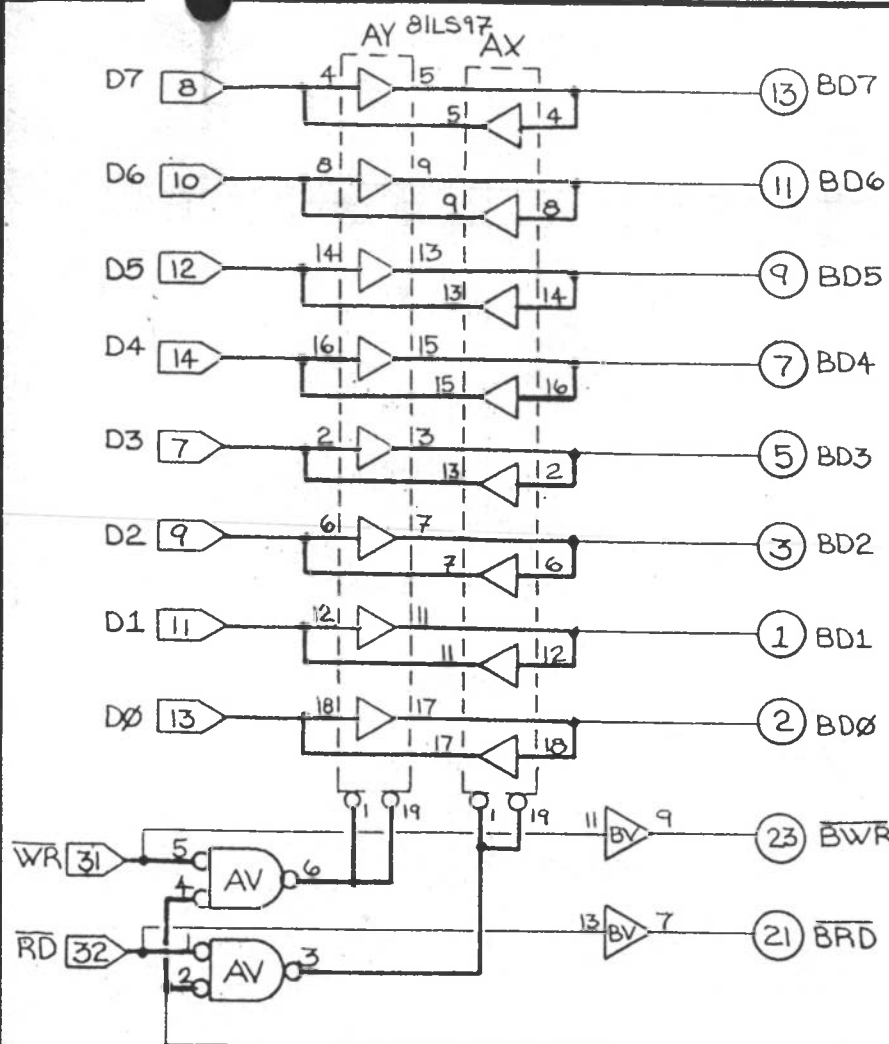
Call out per Model Designation above, specifying:

1. PANELCODER Model Number
2. Pulses Per Revolution
3. VDC
4. Quantity and Delivery Required.



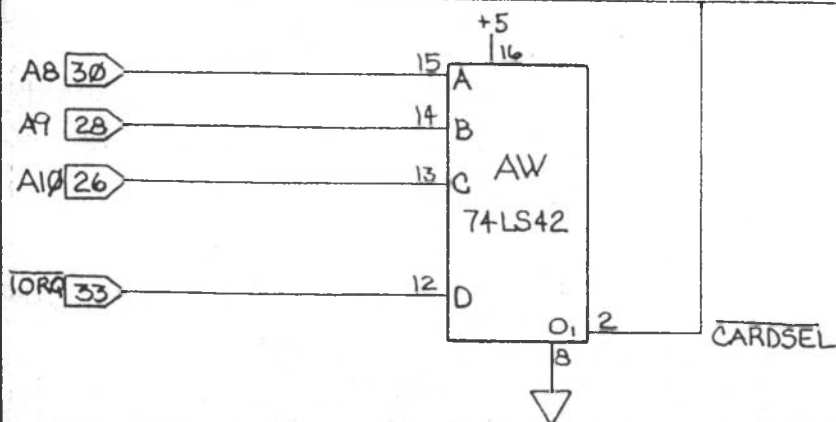
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

TOLERANCES UNLESS OTHERWISE SPECIFIED			
FRACTIONS	DEC	ANGLES	
±	±	±	
APPROVALS		DATE	
DRAWN			
CHECKED			
		SCALE	SIZE
			DRAWING NO.
			11018L1
DO NOT SCALE DRAWING			SHEET 1 of 1



NOTE: BV & BT Pins 1 & 19 are grounded to enable 244's

Dark lines are etches & light lines are wraps.



TOLERANCES UNLESS
OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES
± ± ±

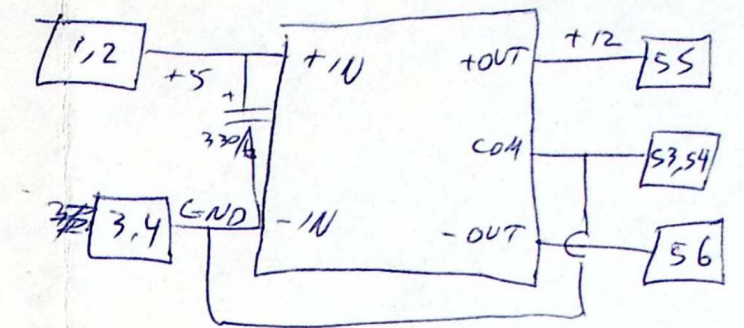
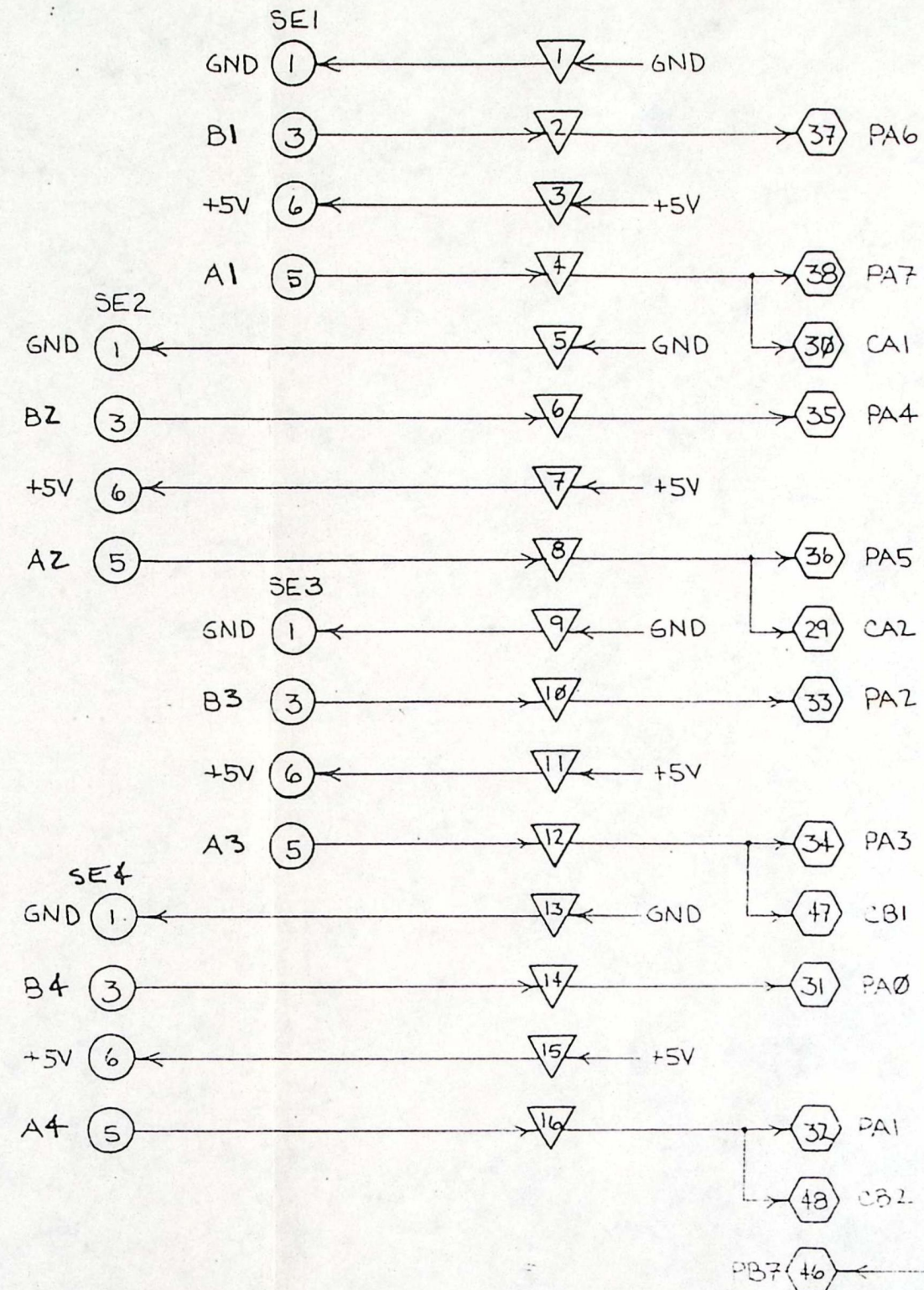
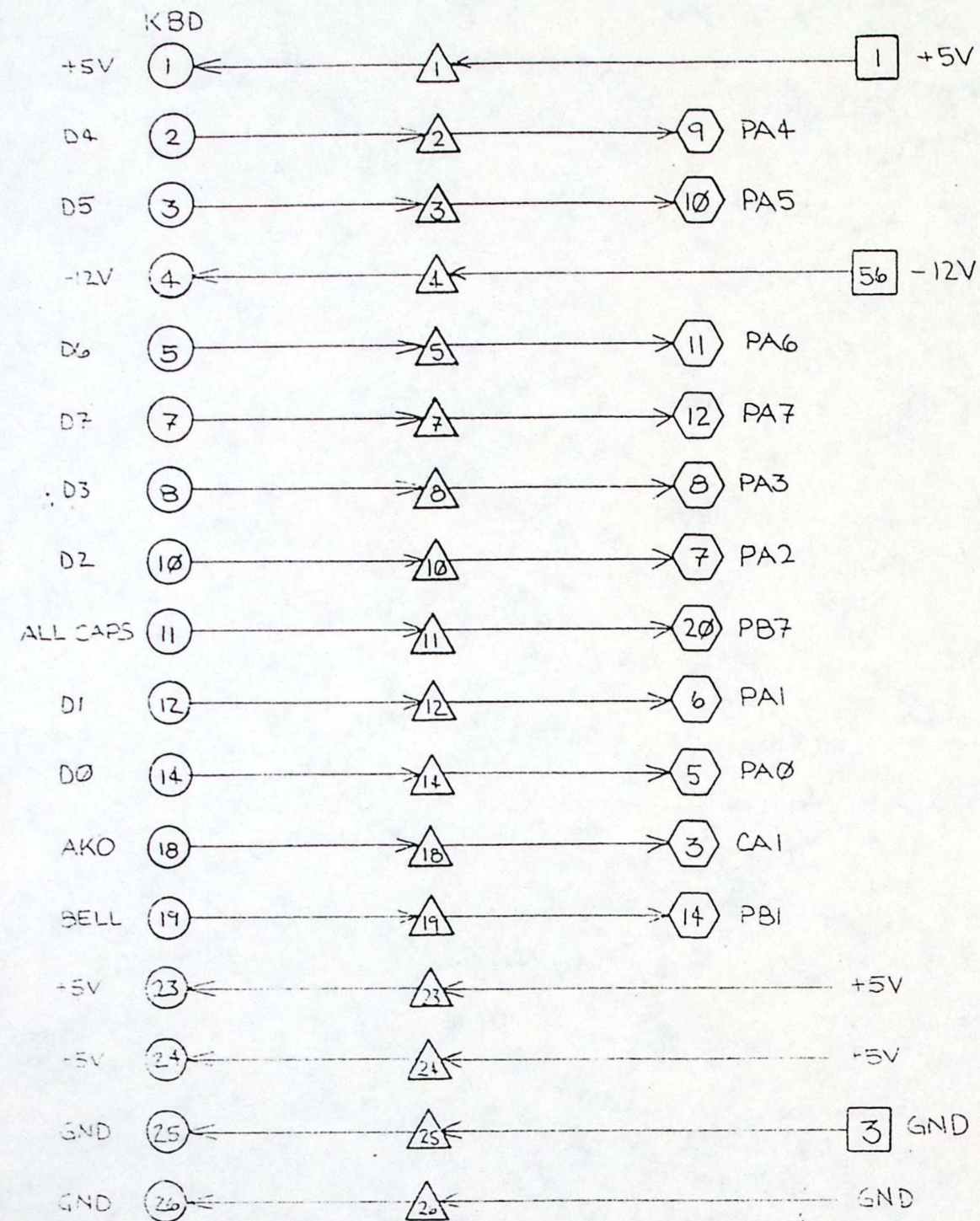
APPROVALS	DATE
DRAWN LPD	11/10/01
CHECKED	

ATA Corp.

COMPUTER IMAGE
CONTROL PANEL
Standard Bus/CIC6 Interface

SCALE	SIZE	DRAWING NO.
		11110L1
DO NOT SCALE DRAWING		SHEET 1 of 1

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



- △ 26 PIN CONNECTOR -B
- ▽ 20 PIN CONNECTOR -A
- CONNECTORS AT KEYBOARD & SHAFT ENCODERS
- ⬡ CONNECTOR TO/FROM 6809 BOARD -C
- STANDARD BUS PINS

TOLERANCES UNLESS OTHERWISE SPECIFIED			
FRACTIONS	DEC	ANGLES	
±	±	±	
APPROVALS	DATE		
DRAWN	1/10/81		
CHECKED			

ATA Corp.

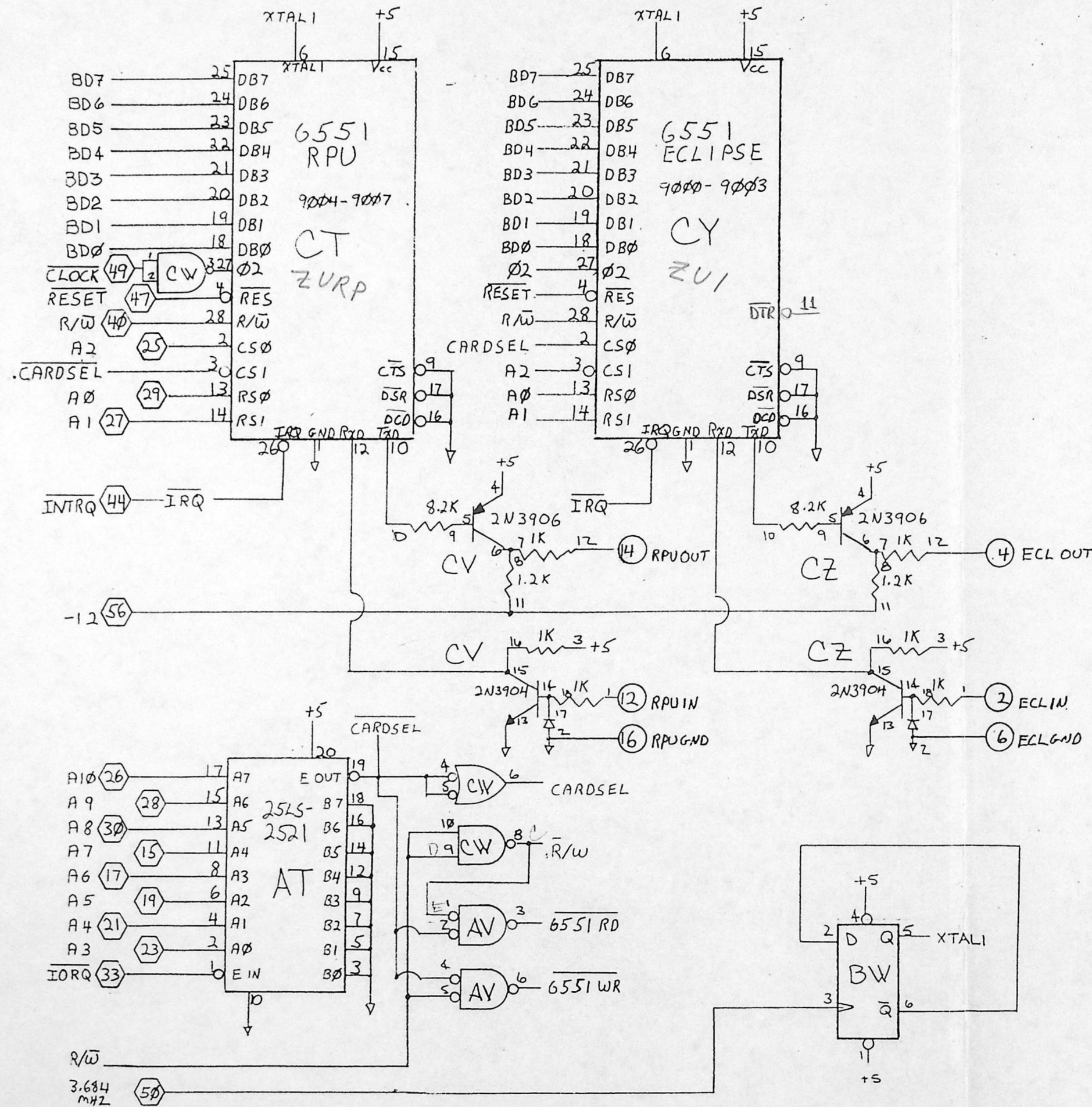
COMPUTER IMAGE
CONTROL PANEL

6809 Aux. Connection Board

SCALE SIZE B DRAWING NO. 10916L1

DO NOT SCALE DRAWING SHEET 1 of 1

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

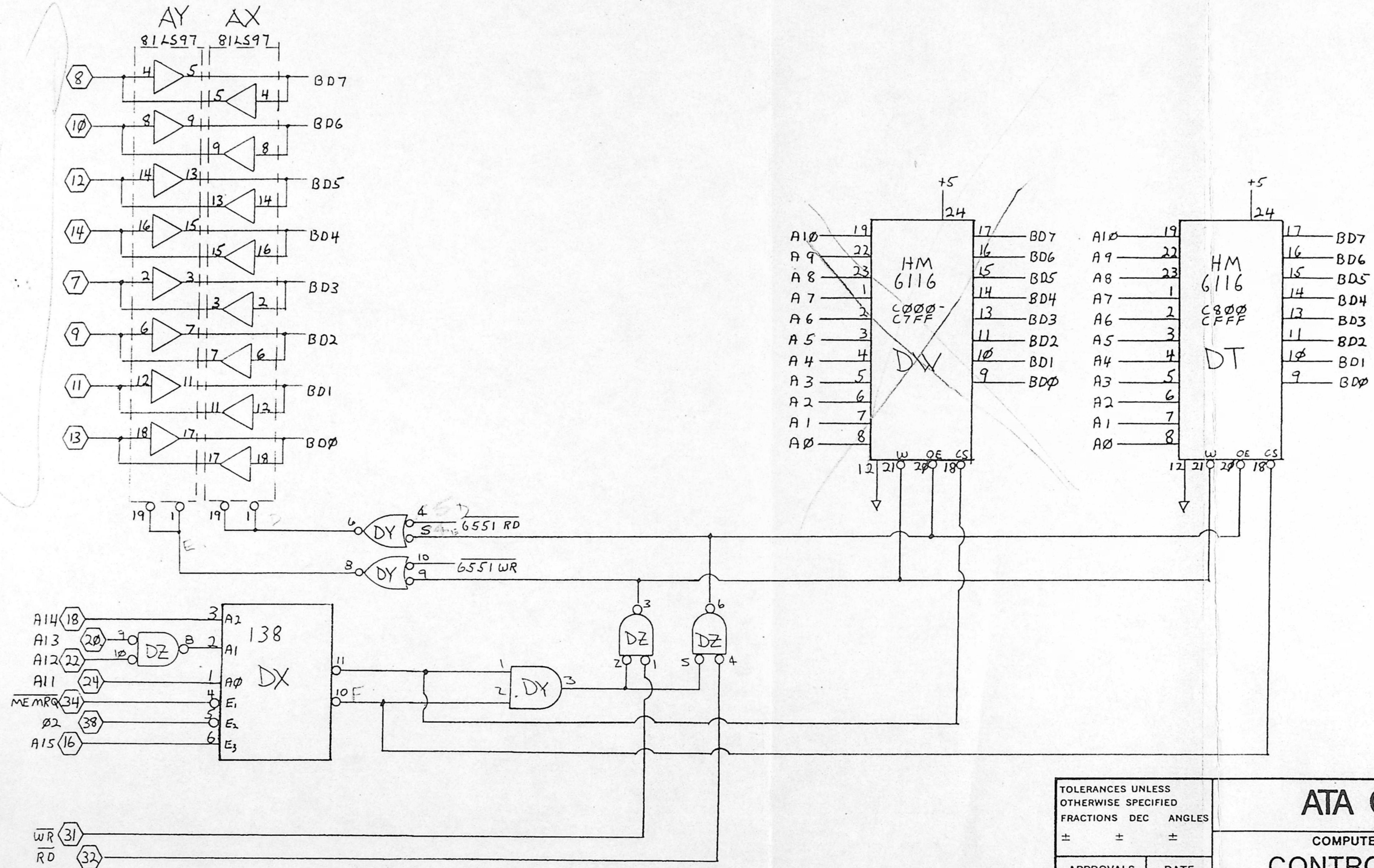


⬡ STD BUS BACKPLANE
 ○ 20 PIN CONNECTOR

NOTE: ON DB25 CONNECTORS PIN 2 = OUTS, 3 = INS & 7 = GNDS

TOLERANCES UNLESS OTHERWISE SPECIFIED			
FRACTIONS	DEC	ANGLES	
±	±	±	
ATA Corp.			
COMPUTER IMAGE CONTROL PANEL			
Eclipse/RPU Communication			
APPROVALS	DATE	SCALE	SIZE
DRAWN DW	9/23/81		B
CHECKED			DRAWING NO.
			11015D1
DO NOT SCALE DRAWING			SHEET 2 of 2

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



TOLERANCES UNLESS
OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES
± ± ±

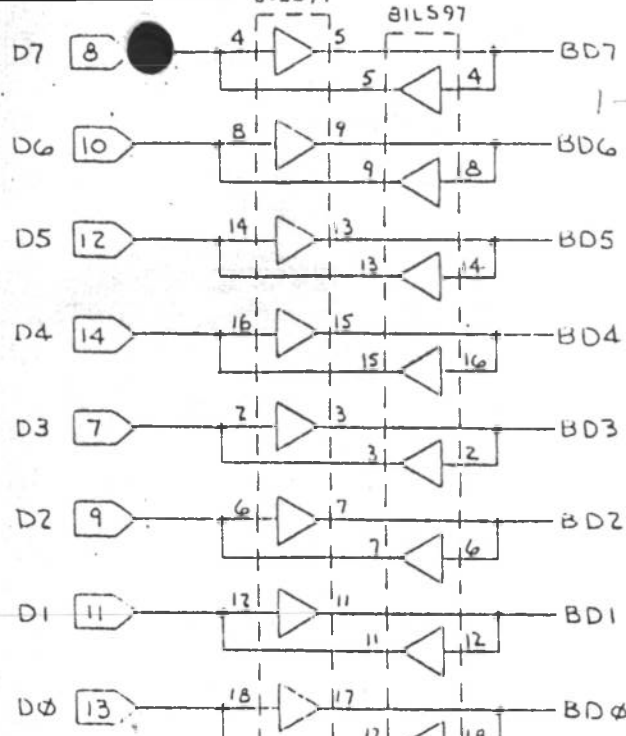
APPROVALS	DATE
DRAWN DW	9/23/81
CHECKED	

ATA Corp.

COMPUTER IMAGE
CONTROL PANEL

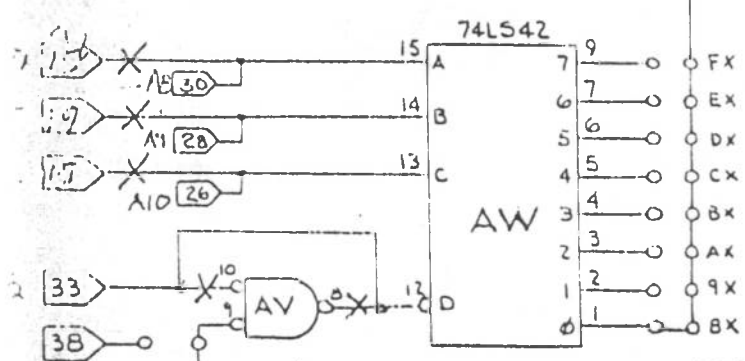
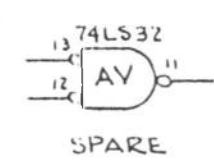
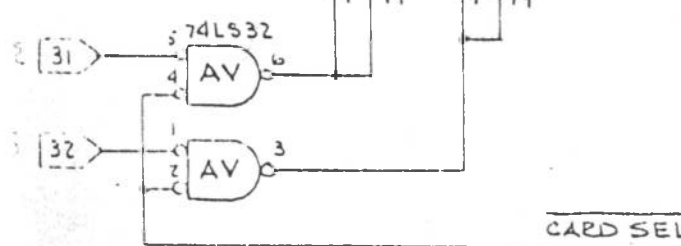
Virtual Ram

SCALE	SIZE B	DRAWING NO. 11015D1
DO NOT SCALE DRAWING		SHEET 1 of 2

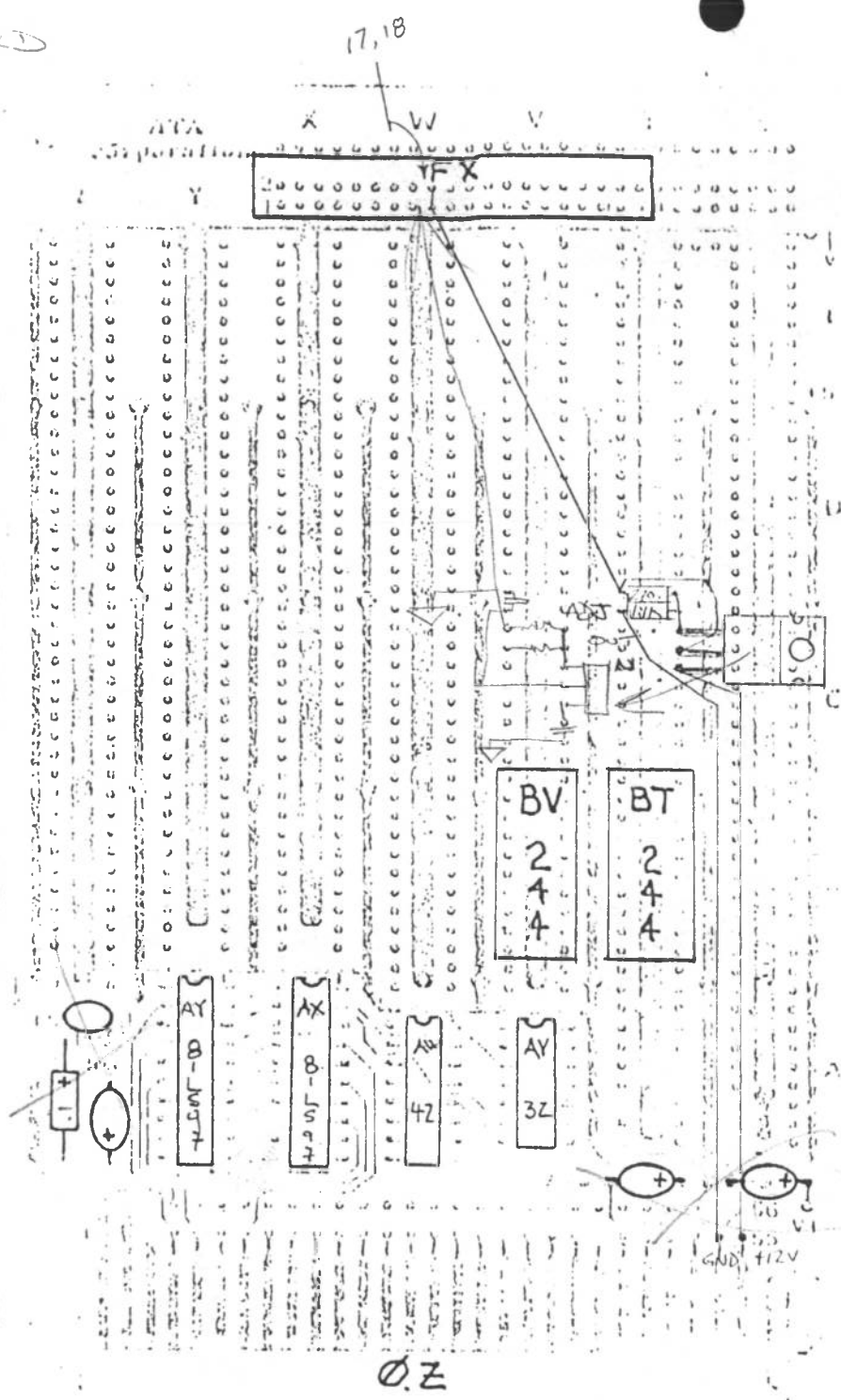


1-74LS244
2-74LS244
2-74LS244
1-74LS42
1-74LS32
1-LM317T
1-270Ω
1-1.1KΩ
2-10μF 25V
1-.1μF
1-10pF
Ww
Solder
Molex 4025 socket
10-17-203Z

8.50.004
CONTENTS
Molex 4025 socket



ATA STD BUS
WIRE WRAP BOARD

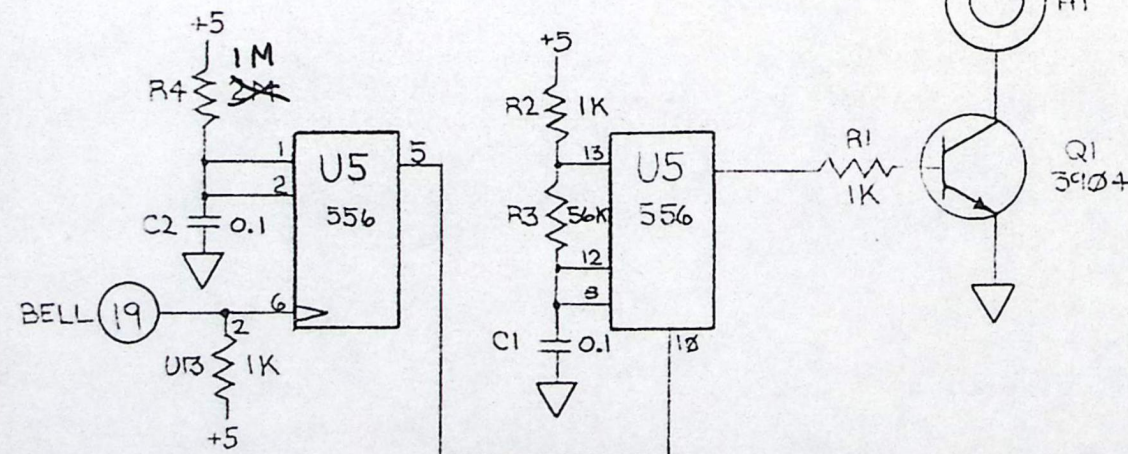
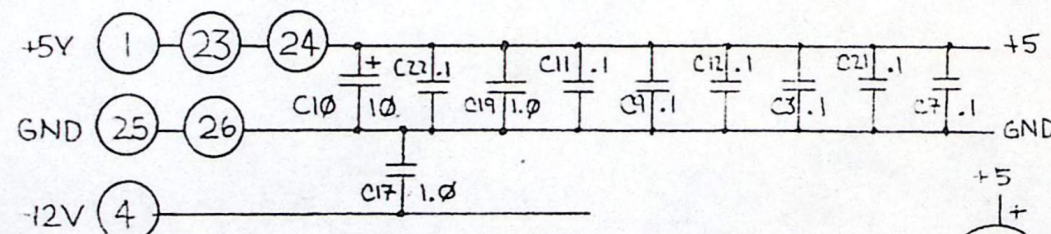
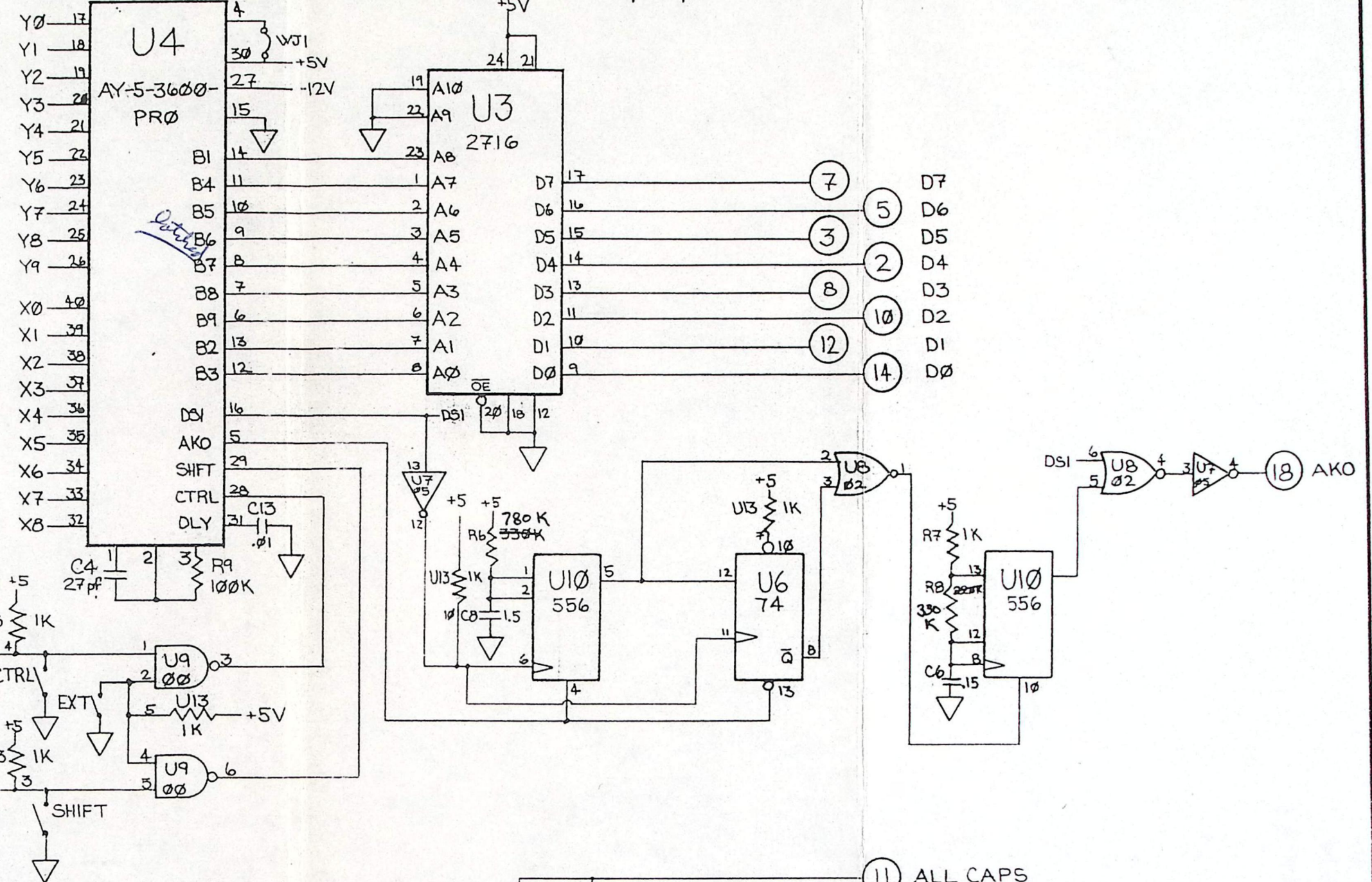
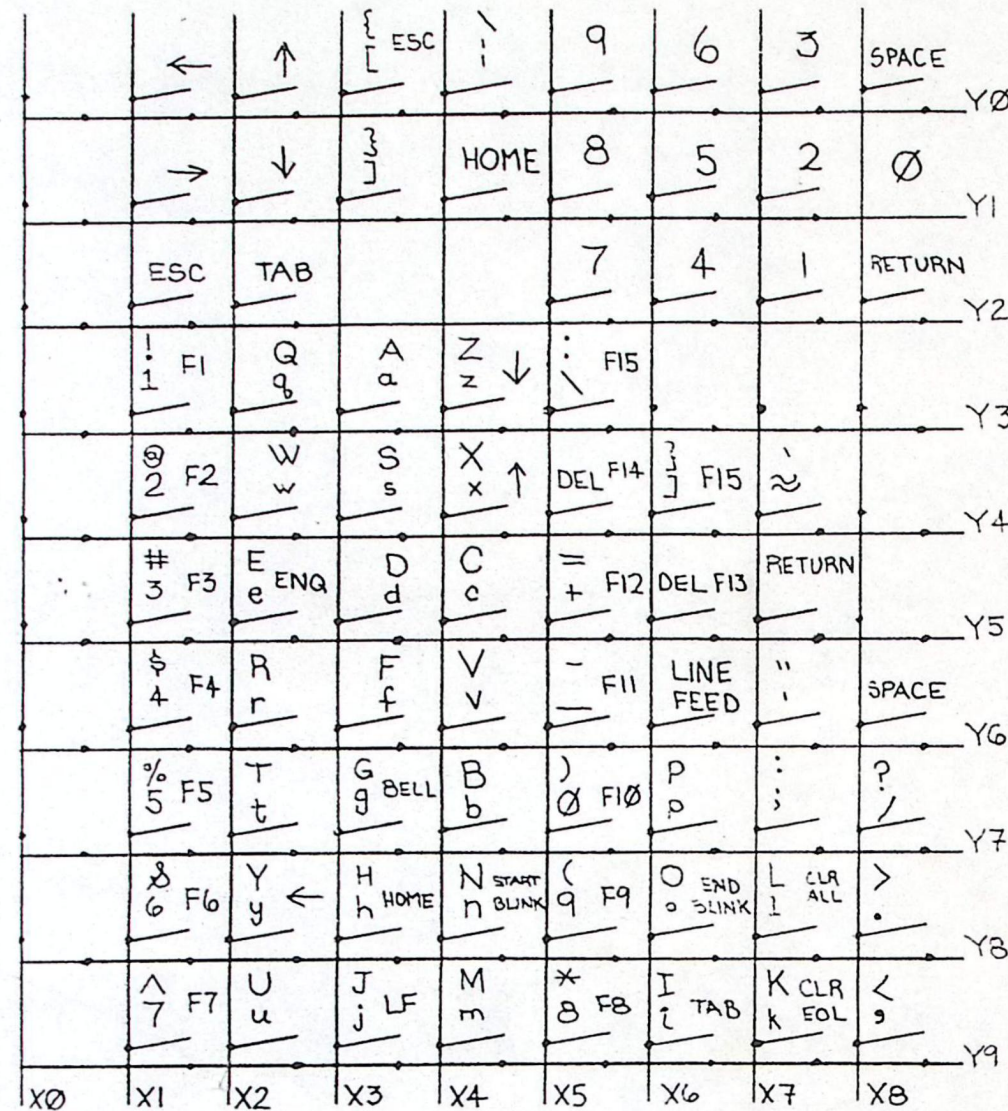


11V
6.3V
REG

MODIFY BOARD
5 CUTS

KEYBOARD PCB SCI-PRO SP-100

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



NOTE: ALL CAPACITOR VALUES IN MICROFARADS UNLESS OTHERWISE NOTED

TOLERANCES UNLESS OTHERWISE SPECIFIED			
FRACTIONS	DEC	ANGLES	
±	±	±	
ATA Corp.			
COMPUTER IMAGE			
CONTROL PANEL			
Terminal Keyboard			
APPROVALS	DATE	SCALE	SIZE
DRAWN LPD	9/18/01		B
CHECKED		DRAWING NO.	10918L1
DO NOT SCALE DRAWING			SHEET 1 of 1

←	→
↓	↑
{	}
[	]
⋮	CEM

ESC	!	@	#	\$	%	&	^	*	(	)	-	=	DEL	
	1	2	3	4	5	6	7	8	9	0	-	+		
TAB	Q	W	E	R	T	Y	U	I	O	P	LINE FEED		RETURN	
CAPS LOCK	A	S	D	F	G	H	J	K	L	;	"	/		
SHIFT	Z	X	C	V	B	N	M	<	>	?	/		SHIFT	
EXT	CONTROL												CONTROL	

7	8	9
4	5	6
1	2	3
RET	Ø	

 COMPUTER IMAGE CORP. DENVER, CO.			
SCALE	NONE	REVISIONS	BY
DATE	1-12-81		
DRN	ASH	CKD	
APVD			
TITLE			NO
SYSTEM IV KEYBOARD			

HM6116P-2, HM6116P-3, HM6116P-4

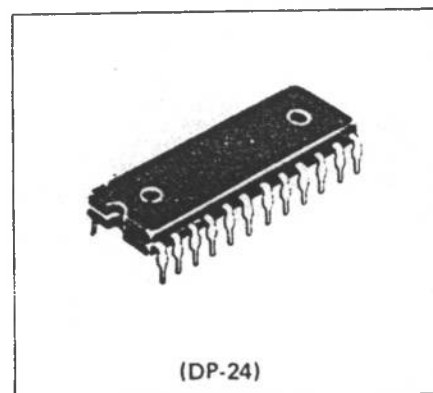
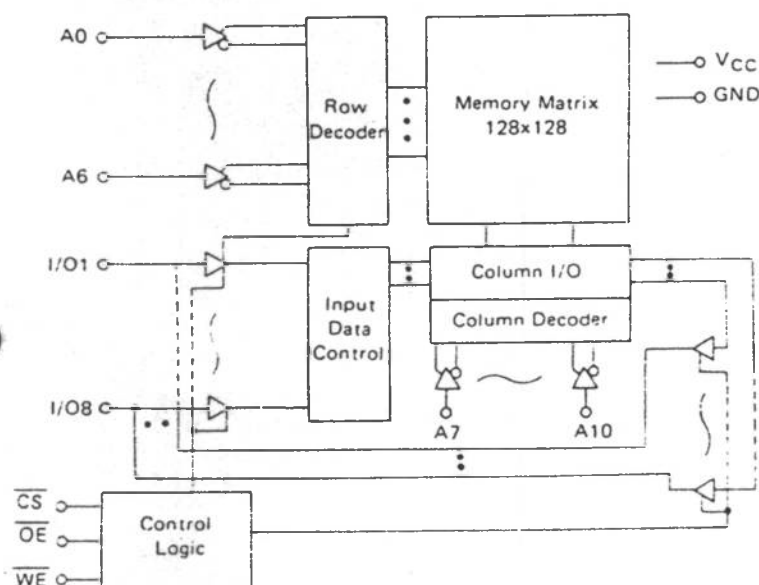
RECEIVED 1981

2048-word X 8-bit High Speed Static CMOS RAM

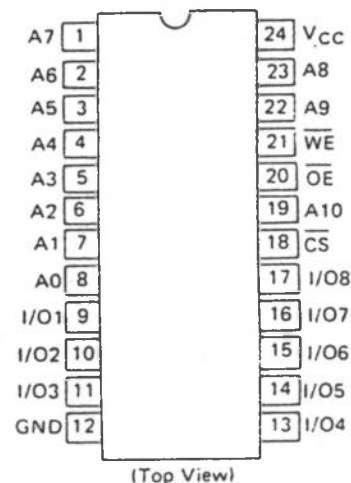
■ FEATURES

- Single 5V Supply and High Density 24 pin Package
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation; Standby: 100 μ W (typ.)
Operation: 180mW (typ.)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

■ FUNCTIONAL BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_{IN}	-0.5 to +7.0	V
Operating Temperature	T_{opr}	0 to +70	$^{\circ}$ C
Storage Temperature	T_{stg}	-55 to +125	$^{\circ}$ C
Temperature Under Bias	T_{bias}	-10 to +85	$^{\circ}$ C
Power Dissipation	P_T	1.0	W

■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1) ~ (3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

HM6116P-2, HM6116P-3, HM6116P-4

RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0 \text{ to } +70^\circ\text{C}$)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	-1.0*	-	0.8	V

* Pulse Width: 50 ns, DC: V_{IL} min. = -0.3V.

DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, GND = 0V, $T_a = 0 \text{ to } +70^\circ\text{C}$)

Item	Symbol	Test Conditions	HM6116P-2			HM6116P-3/-4			Unit
			min.	typ.*	max.	min.	typ.*	max.	
Input Leakage Current	I_{LI}	$V_{CC} = 5.5V, V_{in} = \text{GND to } V_{CC}$	-	-	10	-	-	10	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH} \text{ or } \overline{OE} = V_{IH}, V_{II/O} = \text{GND to } V_{CC}$	-	-	10	-	-	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS} = V_{IL}, I_{II/O} = 0\text{mA}$	-	40	80	-	35	70	mA
	I_{CC1}^{**}	$V_{IH} = 3.5V, V_{IL} = 0.6V, I_{II/O} = 0\text{mA}$	-	35	-	-	30	-	mA
Average Operating Current	I_{CC2}	Min. cycle, duty = 100%	-	40	80	-	35	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$	-	5	15	-	5	15	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V, V_{in} \geq V_{CC} - 0.2V \text{ or } V_{in} \leq 0.2V$	-	0.02	2	-	0.02	2	mA
Output Voltage	V_{OL}	$I_{OL} = 4\text{mA}$	-	-	0.4	-	-	-	V
		$I_{OL} = 2.1\text{mA}$	-	-	-	-	-	0.4	V
	V_{OH}	$I_{OH} = -1.0\text{mA}$	2.4	-	-	2.4	-	-	V

*: $V_{CC} = 5V, T_a = 25^\circ\text{C}$

** : Reference Only

AC CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0 \text{ to } +70^\circ\text{C}$)

AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V - NEC spec 1.8 to 2.2

Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and $C_L = 100\text{pF}$

(including scope and jig)

READ CYCLE

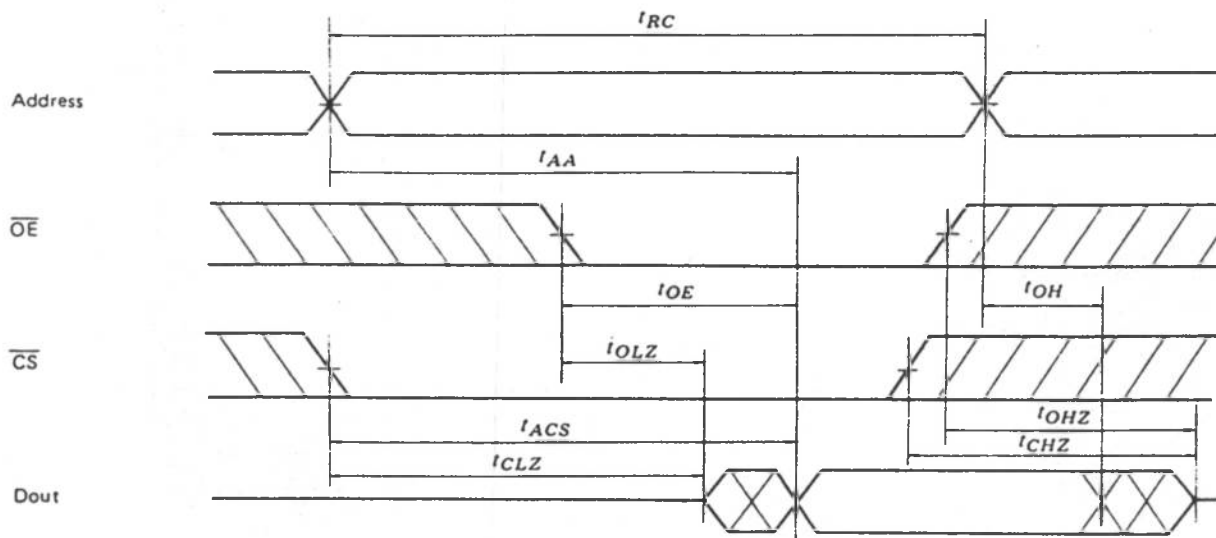
Item	Symbol	HM6116P-2		HM6116P-3		HM6116P-4		Unit
		min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	120	-	150	-	200	-	ns
Address Access Time	t_{AA}	-	120	-	150	-	200	ns
Chip Select Access Time	t_{ACS}	-	120	-	150	-	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	-	15	-	15	-	ns
Output Enable to Output Valid	t_{OE}	-	80	-	100	-	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	-	15	-	15	-	ns
Chip deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	-	15	-	15	-	ns

WRITE CYCLE

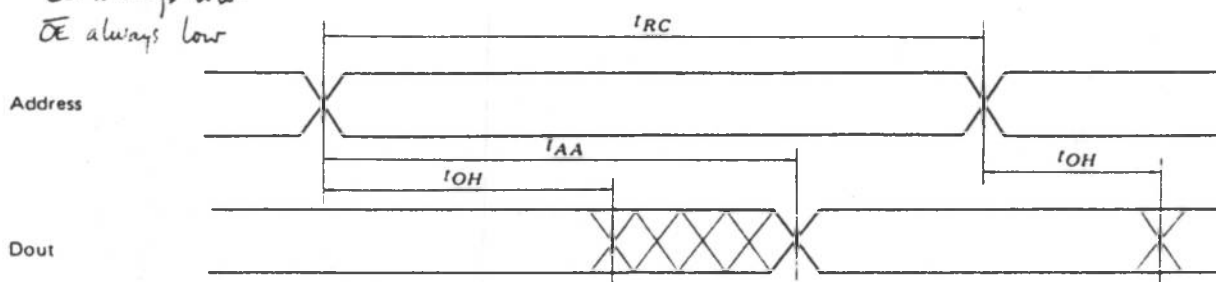
Item	Symbol	HM6116P-2		HM6116P-3		HM6116P-4		Unit
		min.	typ.	min.	max.	min.	max.	
Write Cycle Time	t_{WC}	120	-	150	-	200	-	ns
Chip Selection to End of Write	t_{CW}	70	-	90	-	120	-	ns
Address Valid to End of Write	t_{AW}	105	-	120	-	140	-	ns
Address Set Up Time	t_{AS}	20	-	20	-	20	-	ns
Write Pulse Width	t_{WP}	70	-	90	-	120	-	ns
Write Recovery Time	t_{WR}	5	-	10	-	10	-	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	-	40	-	60	-	ns
Data Hold from Write Time	t_{DH}	5	-	10	-	10	-	ns
Output Active from End of Write	t_{OW}	5	-	10	-	10	-	ns

■ CAPACITANCE ($f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$)

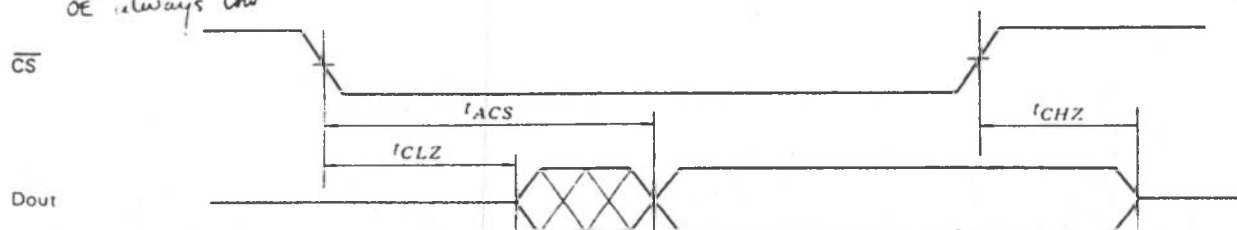
Item	Symbol	Test Conditions	typ.	max.	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0\text{V}$	5	7	pF

● Read Cycle (1) Notes 1, 5

● Read Cycle (2) Notes 1, 2, 4, 5

CS always low
OE always low


● Read Cycle (3) Notes 1, 3, 4, 5

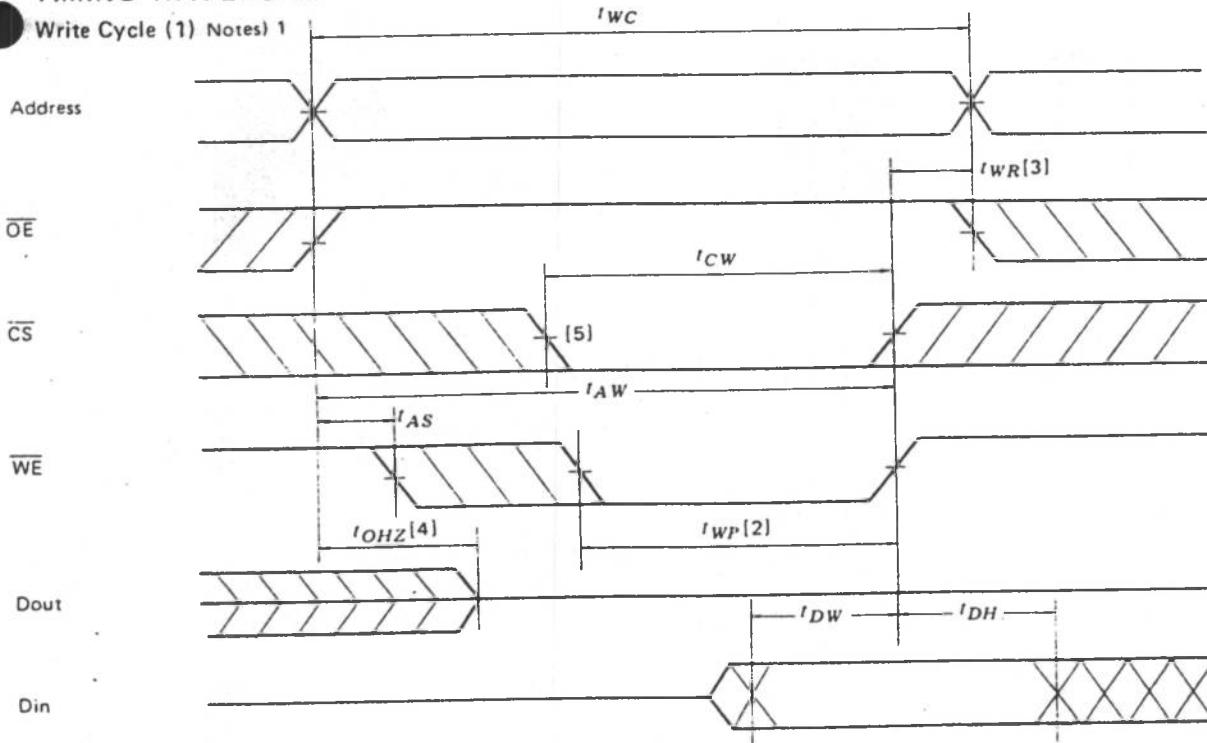
OE always low



- NOTES:
- $\overline{WE}$ is High for Read Cycle.
 - Device is continuously selected, $\overline{CS} = V_{IL}$.
 - Address Valid prior to or coincident with $\overline{CS}$ transition Low.
 - $\overline{OE} = V_{IL}$.
 - When $\overline{CS}$ is Low, the address input must not be in the high impedance state.

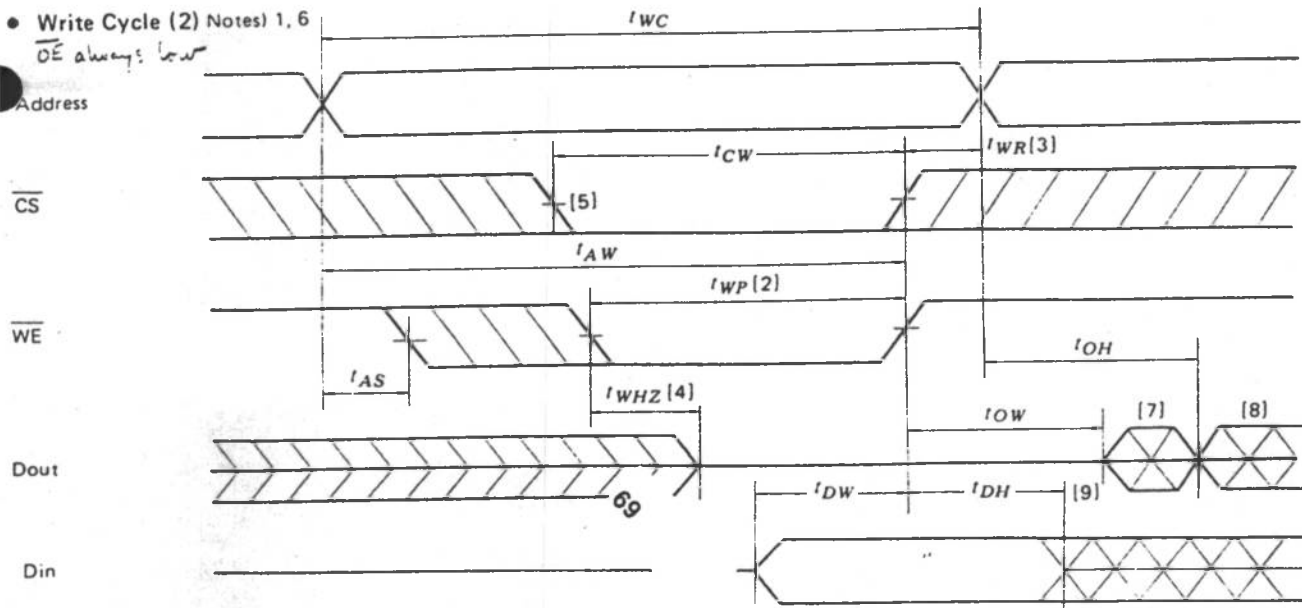
TIMING WAVEFORM

Write Cycle (1) Notes 1



Write Cycle (2) Notes 1, 6

OE always low

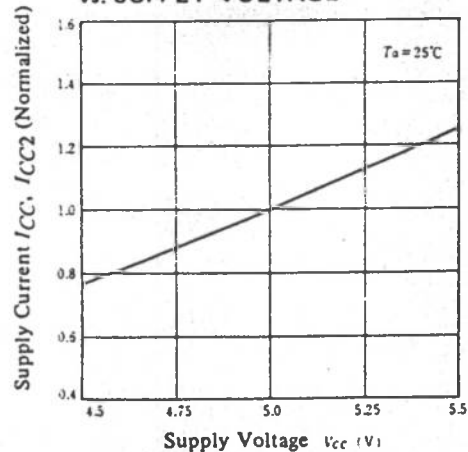


- NOTES:
1. $\overline{WE}$ must be high during all address transitions.
 2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
 3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
 4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$

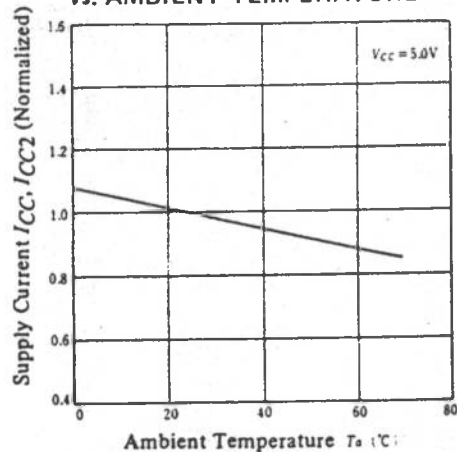
low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.

6. $\overline{OE}$ is continuously low. ($\overline{OE} = I'_{IL}$)
7. D_{out} is the same phase of write data of this write cycle.
8. D_{out} is the read data of next address.
9. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

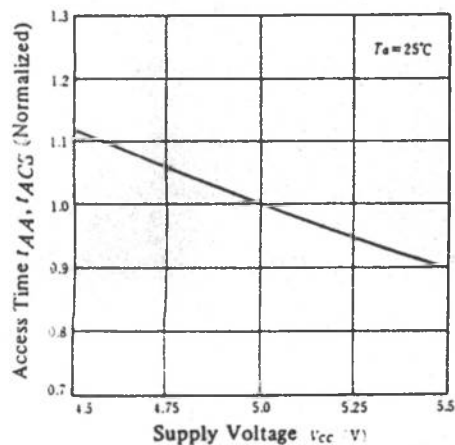
**SUPPLY CURRENT
vs. SUPPLY VOLTAGE**



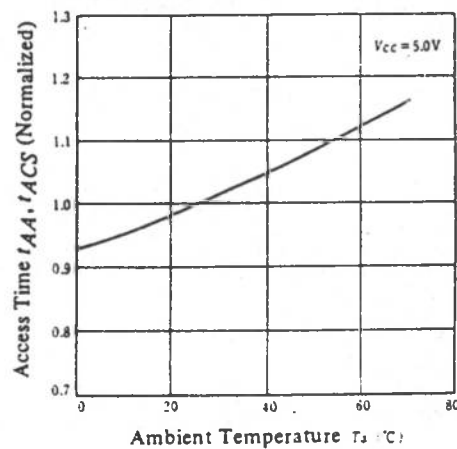
**SUPPLY CURRENT
vs. AMBIENT TEMPERATURE**



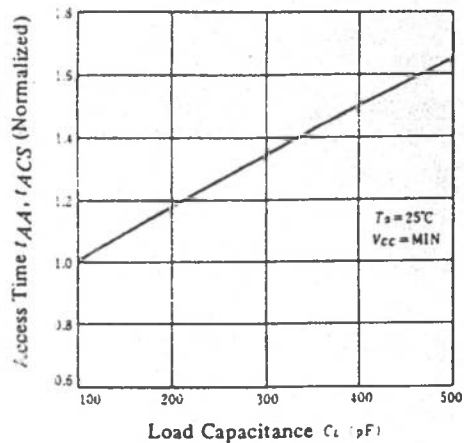
**ACCESS TIME
vs. SUPPLY VOLTAGE**



**ACCESS TIME
vs. AMBIENT TEMPERATURE**



**ACCESS TIME
vs. LOAD CAPACITANCE**



**SUPPLY CURRENT
vs. FREQUENCY**

